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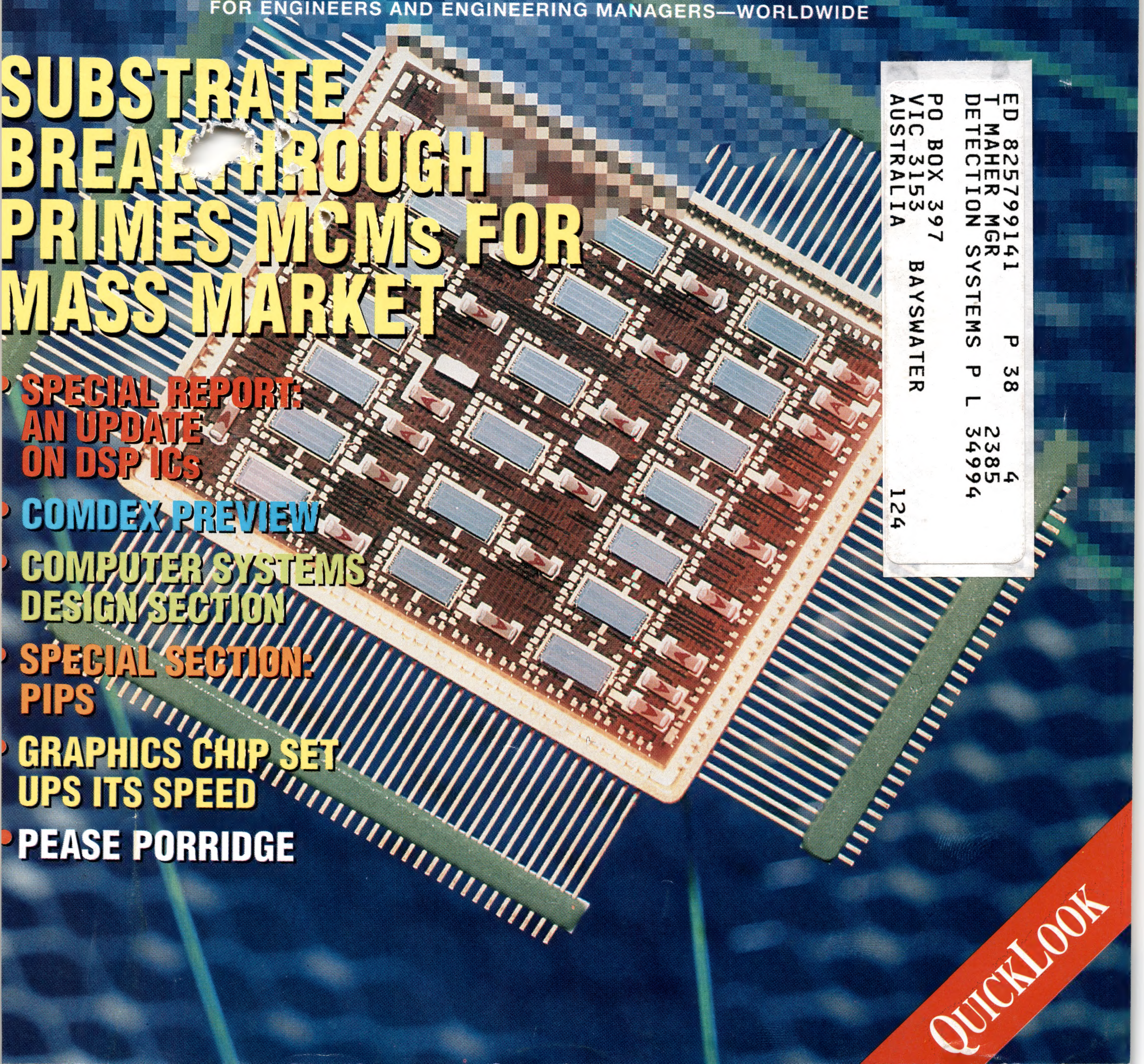

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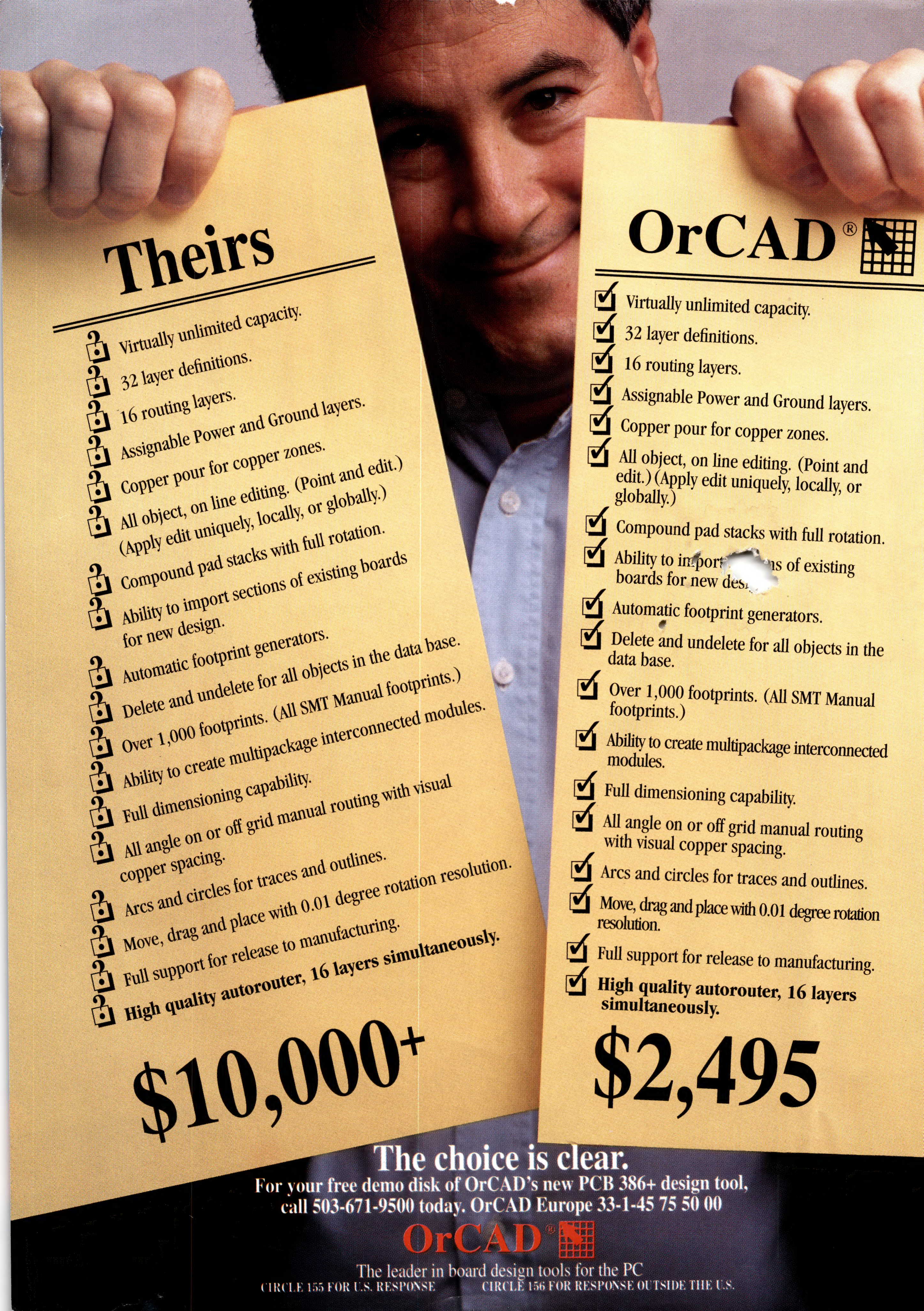

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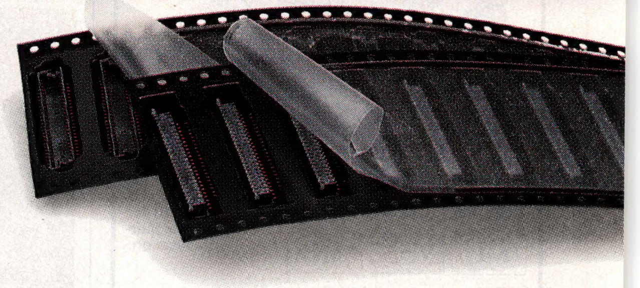

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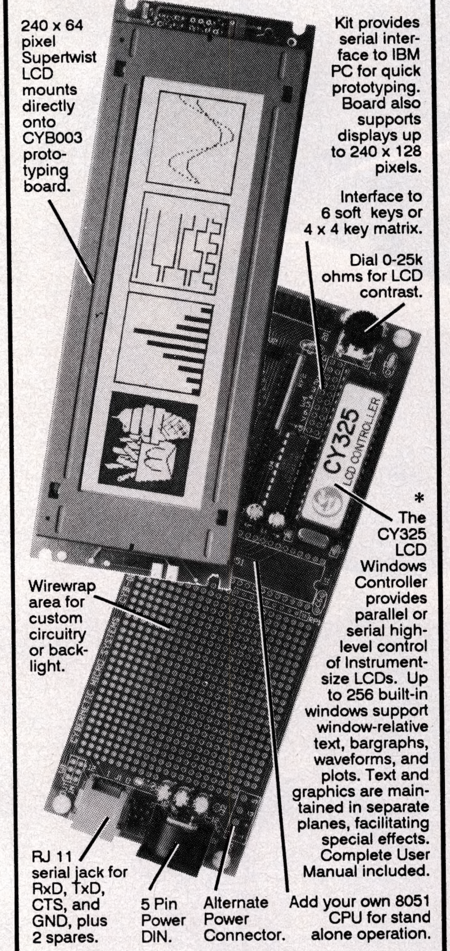
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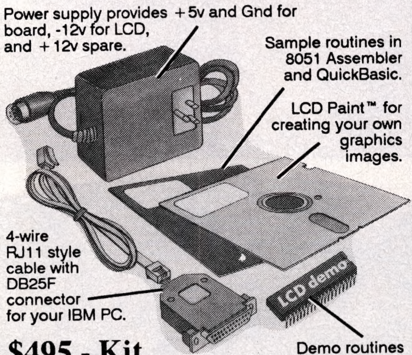
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MISCONCEPTIONS ABOUT PRODUCTIVITY

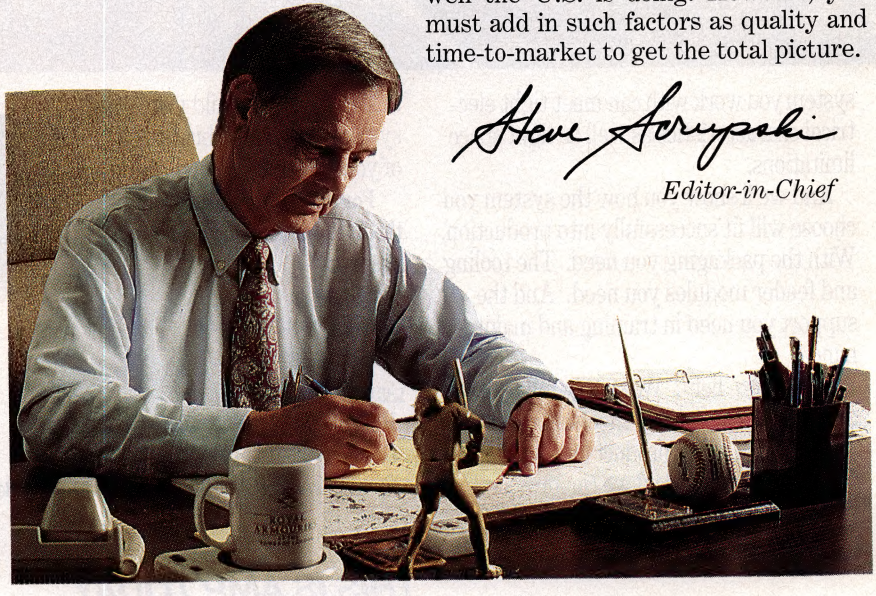
Worker productivity in the United States versus Japan and other countries seems to be under continual attack these days. Certainly, keeping a lid on production costs through design for manufacturability and high employee productivity is a prerequisite for any manufacturing company's long-term ability to compete in international markets. But, despite gloomy reports on productivity that have plagued various industries in the U.S. in recent years, it seems that such gloom and doom are somewhat unfounded. A new study by the consulting firm McKinsey & Co. indicates that U.S. productivity stacks up well against international competitors.

The study covered productivity (output per hour worked) in nine industries: computers, consumer electronics, automobiles, auto parts, metalworking, steel, soaps and detergents, food, and beer. According to the study, as described in The New York Times, U.S. industry is outpacing Japan and Germany in the nine industries taken as a whole: with the U.S. as a base of 100, Germany rates an 83 and Japan a 79. In other words, German productivity overall in these nine industries is 83% that of the U.S. and Japan's is 79%. The U.S. leads in computers, soaps and detergents, beer, and food. Japan leads in steel with a 145, and notched a 124 in auto parts, 119 in metalworking, and 116 in automobiles.

In one segment of the electronics industry—computers—the U.S. also ranked first: The German computer industry's productivity rated an 89 and Japan's a 95. However, in consumer electronics, it's a different story: Japan leads with a score of 115—15% higher productivity than the U.S.—while Germany's productivity in consumer electronics is 62.

Interesting statistics, to be sure, but productivity is not the only contributor to market success. Other factors are just as important, if not more so: quality and time-to-market, to name a couple. In fact, McKinsey & Co. is the same firm that issued the landmark study on the impact of time-to-market on a new product's profitability. When it comes to quality, customer demands seem to be on the rise, and that really isn't reflected in manufacturing productivity. In automobiles, for example, Germany, with a productivity figure of 66 compared with the U.S.'s 100 and Japan's 116, nevertheless has a well-deserved reputation for quality with its Mercedes and BMWs. Yes, they're high-ticket items, but they're also standards-setters for quality (and, depending on your tastes, you might feel the same way about German beer, even though the U.S. beer industry's productivity outdistances Germany's with a score of 100 to 44.)

Productivity numbers are certainly important when trying to measure how well the U.S. is doing. However, you must add in such factors as quality and time-to-market to get the total picture.



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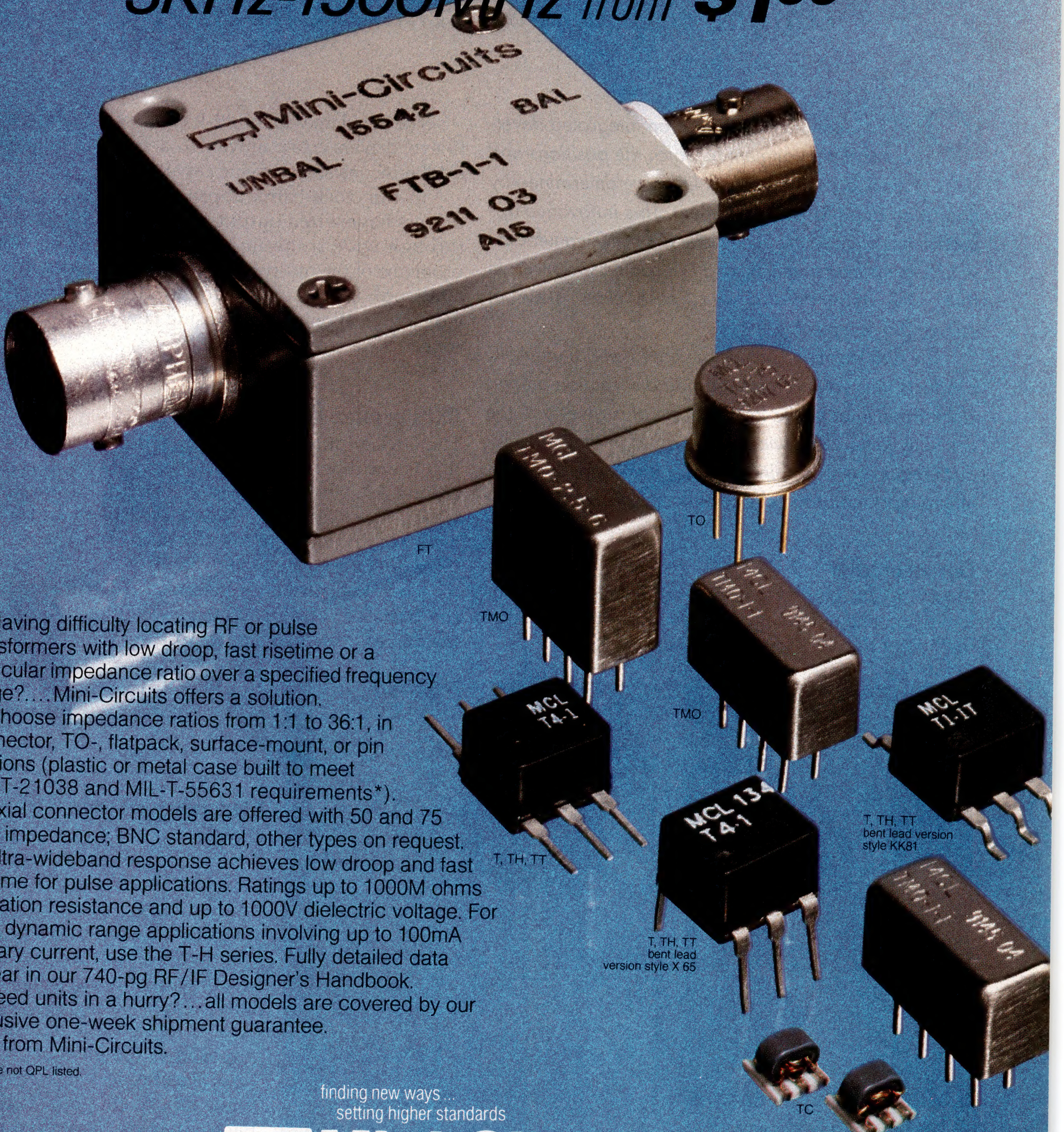

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Minimizing Clock Skew

Unique chip layout technique from OKI

OKI Semiconductor employs an integrated development environment in which the positions and sizes of clock drivers and trunk lines are determined by floor plan and flip-flop placement. This innovative approach has allowed the Sunnyvale, CA ASIC manufacturer to take the lead in minimizing RC loading variances. In fact, OKI guarantees a worst-case clock skew of 1.0 ns; 0.5 ns typical.

The OKI technique, which applies to all 0.8 µm ASIC products, lets you balance loading distribution among clock trunk lines at the layout stage plus gives you the flexibility to handle a wide array of design requirements. Such requirements can include multi-phase clocks, megamacro blocks, a broad choice of floor plans, and more.

Current practice

Most chip designers still address the clock skew problem using one of two approaches: the multi-level tree method or the clock trunk technique.

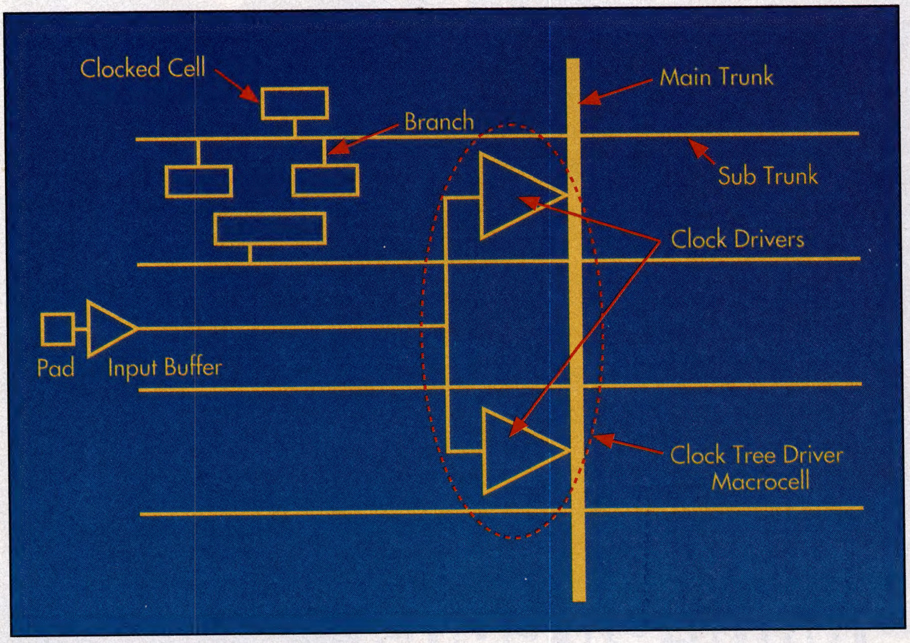

Figure 1. OKI's Clock Tree Structure

The problem with multi-level trees is that the multi-level drivers create unwanted delays and frequently exhibit inconsistent driving capabilities.

In the clock-trunk approach, single-level clock drivers have wired outputs and run all the flip-flops through wide trunk lines. While this can solve the problems of the multi-tree approach, the clock drivers and trunk lines are embedded in the base array, restricting positioning and causing new balance-loading concerns.

OKI's answer: flexible clock trunks

The OKI solution is an automated layout technique that is entirely transparent to the designer. It centers around a flexible, single-level clock trunk approach in which the positions of the clock drivers and trunk lines are driven by the layout software. The advantages of this approach are twofold...

First, the software generates clock trunk lines on the basis of flip-flop distribution, *after* placement, making easy load-balancing possible among the trunk lines. Second, with the OKI solution, you can work with a large variety of design styles used in IC layouts.

Clock driver structure

Figure 1 is a layout showing OKI's unique clock-handling structure. A vertical clock driver – composed of a number of output transistors and having a common output terminal from which trunk lines run horizontally – is placed inside the core area. (The *logical* macrocell, as opposed to the physical structure, is a simple, *one-component* logic model in your netlist.) Each flip-flop connects to a clock trunk via short, minimum-width branch wires.

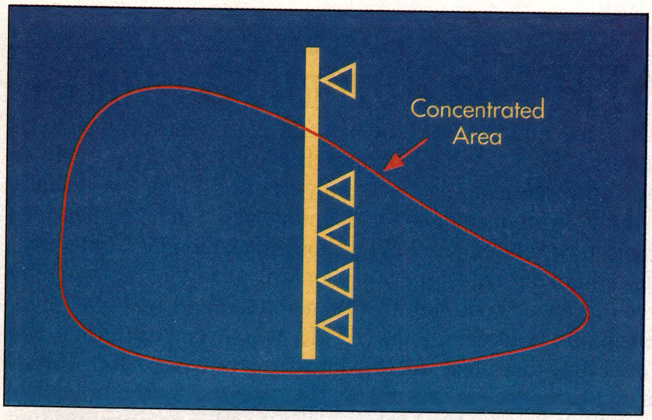

Figure 2. Dynamic Clock Driver Placement

Floor plan placement & clock trunk generation

After a floor planning session using OKI's floor planning tool, you initiate a layout session in which all the components in the design area are automatically placed without regard for clock nets.

The positions and sizes of clock drivers and the sizes of the clock trunk lines are determined by the particulars of the floor plan. The OKI layout software automatically generates an appropriate number of clock trunk lines based upon flip-flop distribution. A higher concentration of trunk lines is dynamically generated (where the lines are needed most) so that loading capacitance and resistance are equally distributed. [See Figures 2 and 3.]

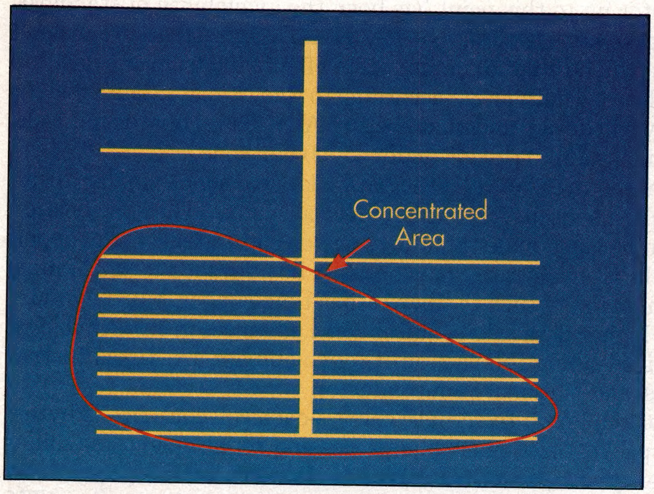

Figure 3. Dynamic Sub-trunk Allocation

Flip-flops are allocated to the trunk lines so that no single line has a greater load. At this point, flip-flop placement is further optimized to reduce layout interconnect. Finally, minimum-length branch nets are routed to each flip-flop, further reducing and balancing clock loading.

Performance benefits

Several factors influence clock performance (speed and skew). These include the driving capability of the clock driver; the fan-out loading capacitance connectable to each clock line; and the parasitic capacitance and resistance existing in the layout interconnect between the clock driver and the individual flip-flops.

To achieve highest performance, OKI has analyzed the range of capacitance and resistance on given die sizes, defining limits for our clock drivers so that the maximum capacitance and resistance on any one clock trunk are not exceeded. These limits, expressed in terms of maximum fan-out loading, are automatically implemented in the new OKI layout technique.

To further assure top performance, routing restrictions, minimizing the length of branch wires, are defined. The cumulative effect of these implementations is to minimize all resistance and capacitance variances. In this way, OKI is able to guarantee minimum clock skew.

The cumulative effect of these implementations is to minimize all resistance and capacitance variances. In this way, OKI is able to guarantee minimum clock skew.

Exceptional test results

OKI has conducted numerous studies on 0.8 µm designs using the new layout technique. In each case, the RC circuits of the clock nets were extracted and clock skew checked and verified by an HSPICE* circuit simulator. The results were excellent. In all the tests, the greatest skew obtained was 0.47 ns – a showing that further confirms the value of the OKI technique in which the positions of clock drivers and clock trunk lines are flexibly generated. ■

*A trademark of Meta-Software, Inc.

For an application note and a copy of the complete technical paper treating the OKI method of reducing clock skew, call (800) OKI-6388, and ask for Literature Package # 017. For more information from an OKI engineer, call Steve Lapham, (408) 737-6337.

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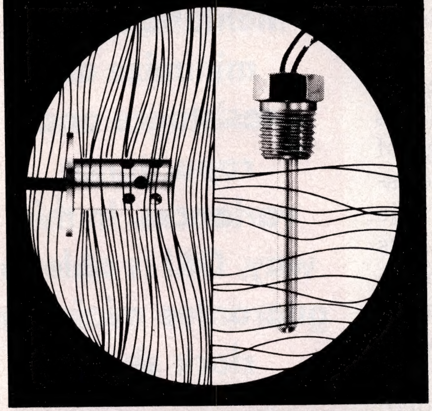

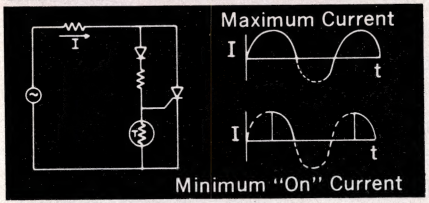

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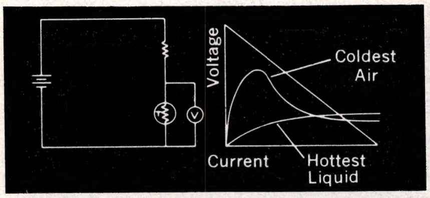

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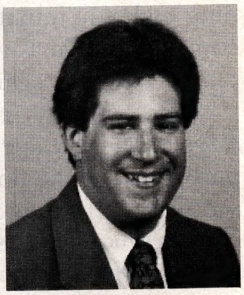
BANK ON ATM FOR FUTURE NETWORKS

It's no secret that the amount of data passing over networks links is creating bottlenecks. So, what's to blame? Basically, all signs seem to point to current and forthcoming data-hungry applications, especially those passing audio, video, images, and animation. Such applications include multimedia, teleconferencing, and even those in the medical industry.

To combat this onslaught of data, designers are looking at several networking alternatives—ways to increase the amount of transmitted and received data. One choice is asynchronous transfer mode (ATM), which facilitates moving large chunks of data over long distances. ATM's data-transfer rate is 155 Mbits/s over either single- or multi-mode fiber, or unshielded twisted-pair copper. The technology will eventually be applied to both business- and consumer-product communications. What's more, companies like Fujitsu and AT&T are designing wide-area ATM networks.

Although the ATM technology won't be in the mainstream for a few years, products will probably start to appear in the latter half of 1994. National Semiconductor Corp., Santa Clara, Calif., for example, recently demonstrated a working ATM board at the Interop trade show.

"1994 will be a very exciting year for ATM because that's when the initial products will hit the market," says Shekar Rao, chairman of the ATM Forum's Market Awareness and Education Committee (Rao also is vice president of marketing at Efficient Network Technology in Dallas, Texas). The ATM Forum was formed to govern the ATM specification and handle communications between the 350 member companies that represent a cross-section of the entire industry. The ATM Forum, headquartered in Mountain View, Calif., can be reached at (415) 962-2585.



RICHARD NASS
COMPUTER SYSTEMS

"The negating factor up to this point has been the availability of standard-product ICs. During the next 18 to 24 months, the ATM infrastructure will fall into place and people will be able to communicate effectively from one desktop to another over ATM-based networks," according to Rao. He says that Efficient Network Technology will design and manufacture ATM-based boards for desktop systems, expecting them to sell for under $1000 per node.

An ATM solution requires an adapter card at each node, similar to an Ethernet setup. It also needs an ATM hub for a local system. The specification permits copper wire because many buildings are already wired with copper. With fiber, though, the transfer rate can eventually be upgraded to 622 Mbits/s and beyond. Thus, many may turn to fiber rather than copper, but they must also realize that the higher data rate requires some advances in IC technology. Among the companies leading the pack in IC development are Texas Instruments, Dallas, Texas, and National Semiconductor.

The ATM protocol employs a fixed byte count—each cell contains 53 bytes. This relatively low packet size lowers the processing requirement and eliminates almost all latency in a packet transmission. In addition, the packets can be prioritized. To maintain compatibility with existing standards, the ATM protocol was modeled after the Scalable Optical Network (Sonet) specification. Sonet defines the transportation and management of digital data.

FDDI, which stands to be replaced by ATM, is the current state of the art for high-end networks. Running at 100 Mbits/s, FDDI differs from ATM in that it's a shared technology. In other words, when another party joins the network, the performance is degraded: The more people crowding onto the line lessens the amount of bandwidth available to each user. With ATM, the full bandwidth is always available. Features that make FDDI attractive are that it's available now and it offers an upgrade path to ATM. Upgrading simply requires an ATM card at each terminal and an ATM switch.

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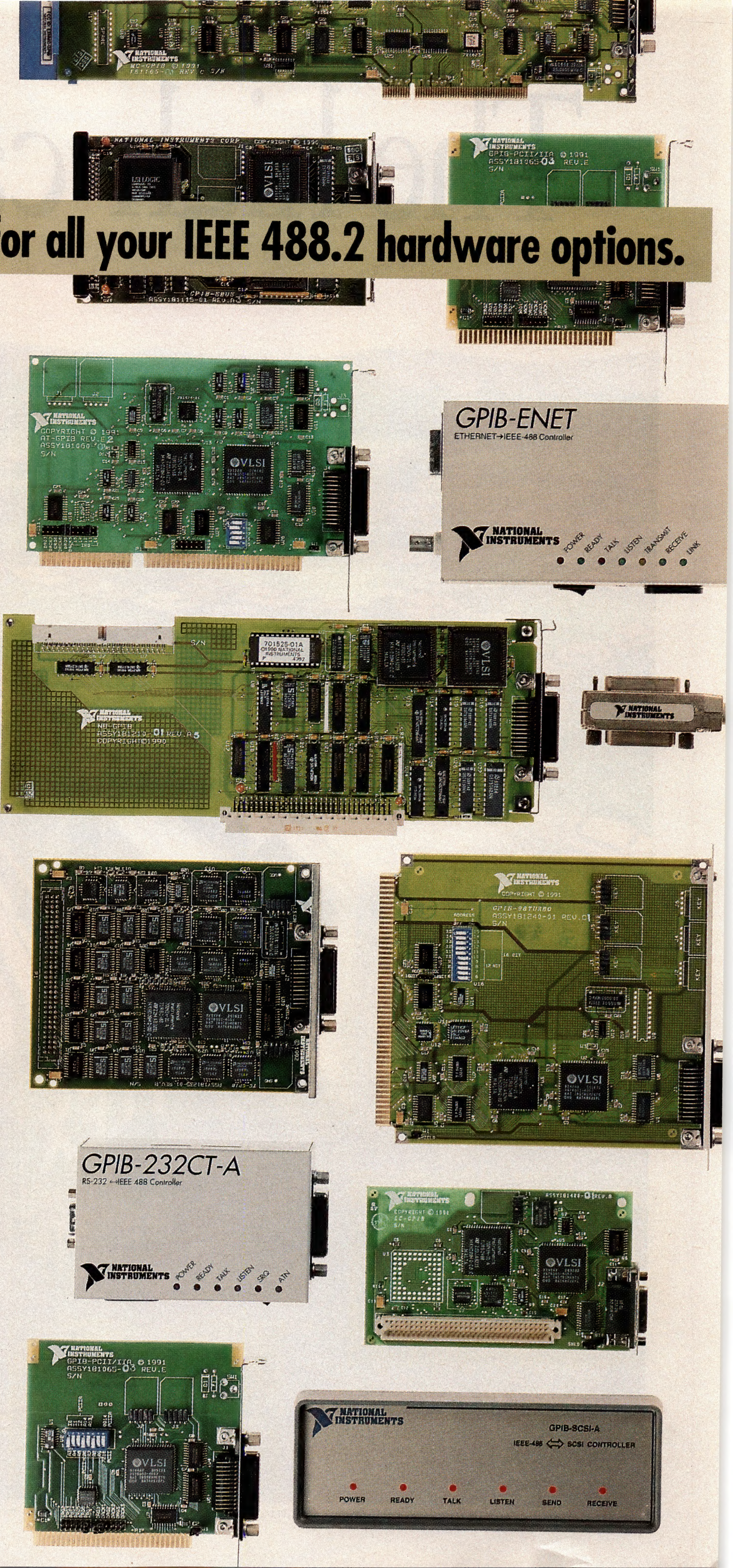

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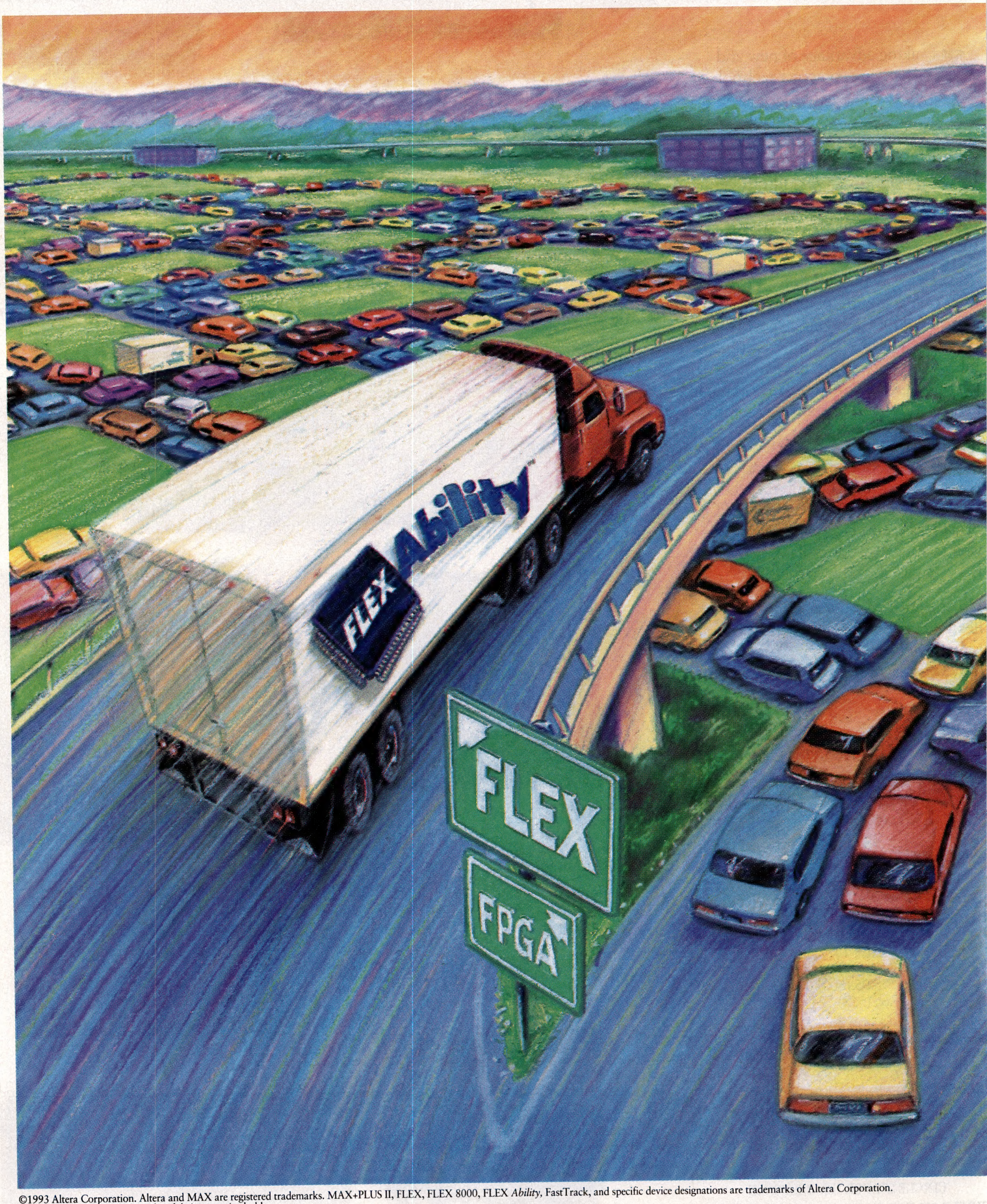

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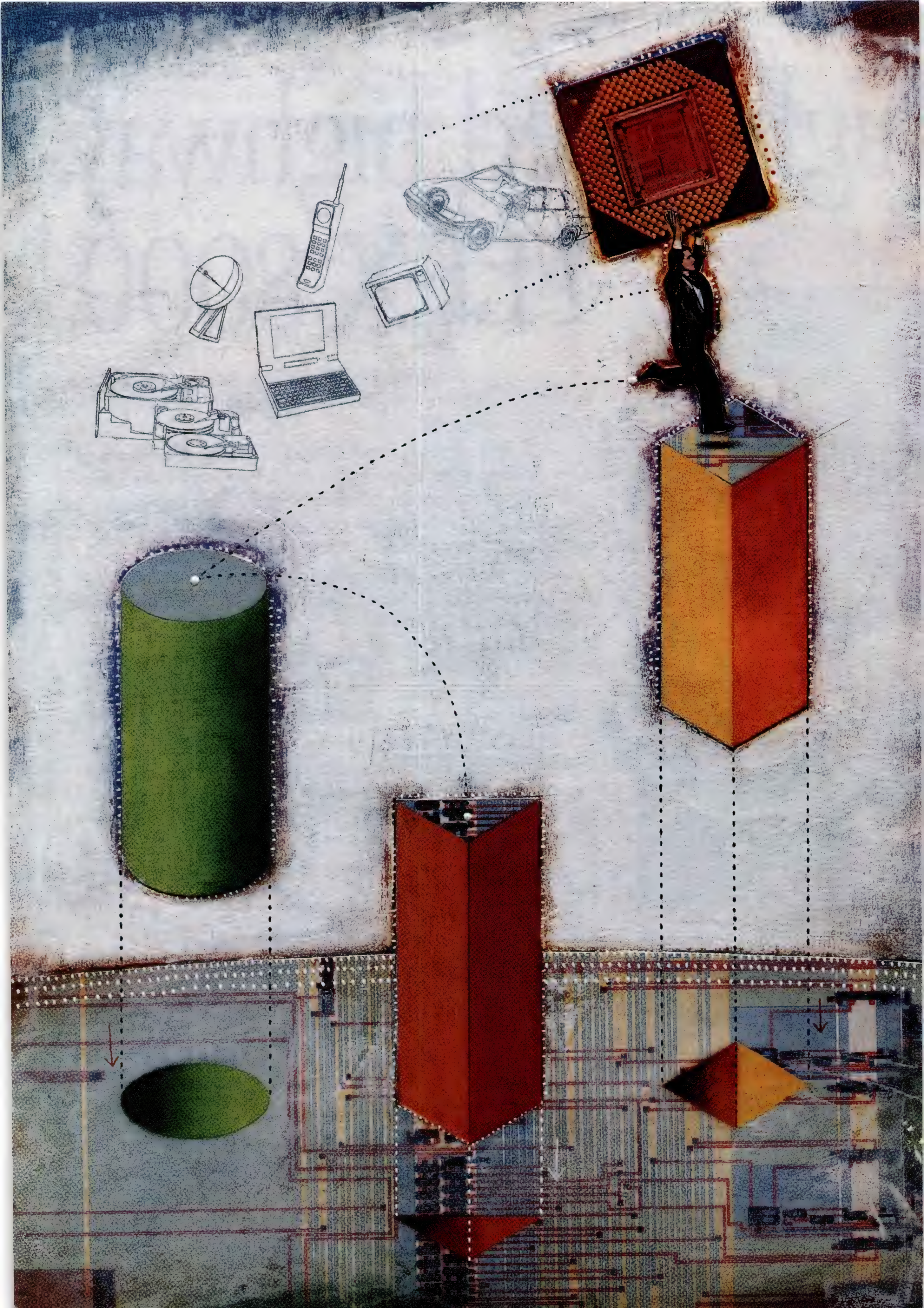

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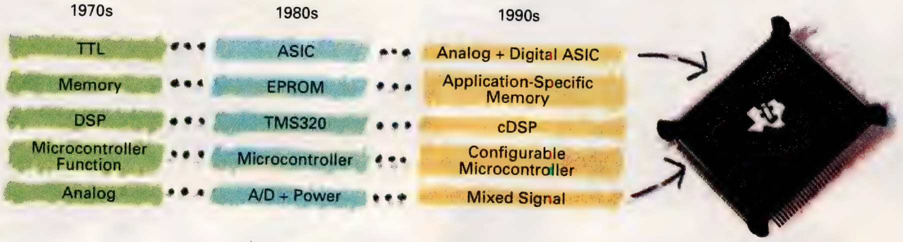

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TECHNOLOGY NEWSLETTER

TASK FORCE STUDIES CFC REPLACEMENT PROCESSES

Small and mid-sized electronics companies nervously anticipating the 1996 phase-out of chlorofluorocarbons (CFCs) for cleaning solder flux from pc boards and other devices may find an answer to their problems in a research program sponsored by the U. S. Federal Advanced Research Projects Agency (ARPA). A team of government, industry, and university scientists and engineers has been formed to evaluate substitute cleaning technologies for their applicability in different manufacturing scenarios. As of now, no single replacement technology is a "drop-in solution" for the wide range of processes that use CFC cleaning, says Dr. Laura Turbini, the Georgia Institute of Technology engineering professor who heads the team. The team will first study processes that have matured to commercial viability, including semi-aqueous and aqueous detergent cleaners, and water-soluble fluxes. In the future, it will turn its attention to less mature techniques, such as low-solids/no-clear fluxes and controlled-atmosphere soldering. The two-year effort will make information dissemination a priority by publishing a newsletter, setting up an electronic bulletin board, and conducting tutorials over broadcast satellite. The 1996 deadline is a real one because according to the Montreal Protocol signed in 1987, production on CFCs, which are thought to be responsible for depleting the ozone layer, will end in in 1996. In addition to Georgia Tech, other participants come from the U. S. Army MICOM; the U. S. Naval Air Warfare Center at China Lake, Calif.; the U. S. Air Force's Rome Laboratory; NASA's Goddard Space Flight Center; Martin-Marietta; Raytheon; Hughes Aircraft; Texas Instruments; and Motorola. Contact Laura Turbini at (404) 853-9073. *JS*

SILICON ICS TO CUT NOISE POLLUTION

Signal-processing ICs and highly efficient power amplifiers developed by Harris Semiconductors, Melbourne, Fla., are expected to aid in the war on noise pollution. Harris and Noise Cancellation Technologies (NCT), Stamford, Conn., will jointly develop and manufacture proprietary silicon ICs that can implement NCT's active noise-reduction technology. The basic noise-cancellation technology involves using a microphone to pick up the noise sources, digitizing the noise signals, and then applying those signals to a DSP IC. The processor analyzes the signal in real time and "calculates" a train of digital words equal and opposite to the noise signal. This so-called "anti-noise" signal is converted to analog form, amplified for both amplitude and power levels, and applied to one or more loudspeakers whose outputs cancel (null out) the original noise. Harris brings its analog signal-processing IC techniques to the project along with its on-chip high-frequency (1-MHz) power pulse-width-modulation (PWM) IC process. Harris' wide-band op amps, multiplexers, and data converters will handle the analog signals between the microphone and the DSP circuit, and between the DSP circuit and the power amplifier. The PWM circuits can be used in class-D switching power amplifiers with efficiencies topping 90%. *FG*

PARTNERSHIP TARGETS IC-PACKAGE INSPECTION

Due to the lack of a comprehensive approach for IC-package inspection, Applied Intelligent Systems Inc. (AISI), Ann Arbor, Mich., and IntelliVision Ltd., Seoul, South Korea, are pooling their resources to come up with a solution. At present, numerous partially automated means of inspecting packages exist for print legibility, lead positions, and lead coplanarity. These methods, however, must be augmented by human visual inspection. AISI's latest generation of vision computers will be combined with newly developed lighting techniques and vision-analysis approaches to integrate vision into the semiconductor-packaging process. Complete IC inspection may require dozens of different lighting and vision-processing combinations to cover the full spectrum of device types. AISI's all-software approach to algorithm development, coupled with the power of massively parallel processors, is expected to help make this possible. For information, call AISI at (313) 995-2035. *DM*

TOOLSET OPTIMIZES POWERPC 603 PROCESSOR

Five new software tools should help developers take advantage of the PowerPC 603 microprocessor, whose low power consumption and low cost suit it for notebooks, desktop computers, and embedded applications. From Motorola Inc.'s Microprocessor Division, Austin, Texas, the Software Development Package includes optimizing C and Fortran compilers, a source-level debugger, and an architectural simulator that enables developers to create and test software for the 603 processor before

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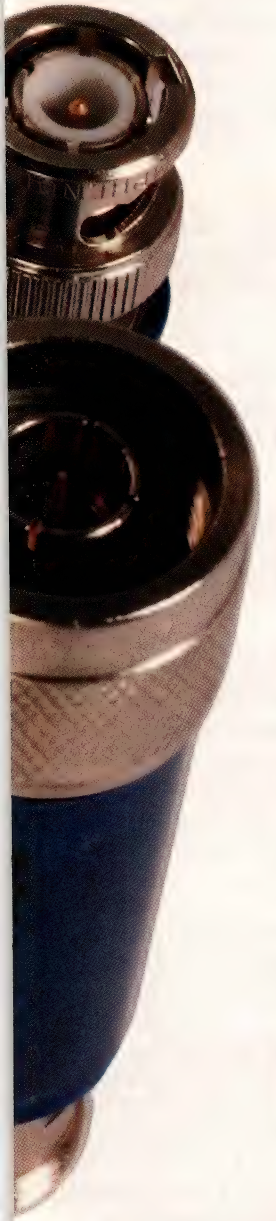


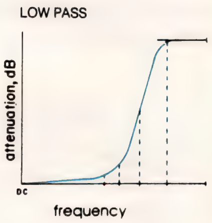
low pass, Plug-in, dc to 1200MHz

Model No.	Passband MHz loss < 1dB	Stopband, MHz	
		loss > 20dB	loss > 40dB
★LP-5	DC-5	8-10	10-200
★LP-10.7	DC-11	19-24	24-200
★LP-21.4	DC-22	32-41	41-200
★LP-30	DC-32	47-61	61-200
★LP-50	DC-48	70-90	90-200
★LP-70	DC-60	90-117	117-300
★P-90	DC-81	121-137	167-400
★LP-100	DC-98	146-189	189-400
★LP-150	DC-140	210-300	300-600
★LP-200	DC-190	290-390	390-800

Model No.	Passband MHz loss < 1dB	Stopband, MHz	
		loss > 20dB	loss > 40dB
★LP-250	DC-225	320-400	400-1200
★LP-300	DC-270	410-550	550-1200
★LP-450	DC-400	580-750	750-1800
★LP-550	DC-520	750-920	920-2000
★LP-600	DC-680	840-1120	1120-2000
★LP-750	DC-700	1000-1300	1300-2000
★LP-800	DC-720	1080-1400	1400-2000
★LP-850	DC-760	1100-1400	1400-2000
★LP-1000	DC-900	1340-1750	1750-2000
★LP-1200	DC-1000	1620-2100	2100-2500

Price, (1-9 qty), all models: plug-in $14.95, BNC $32.95, SMA $34.95, Type N $35.95

LOW PASS



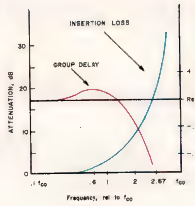
Surface-mount, dc to 570MHz

SCLF-21.4	DC-22	32-41	41-200
SCLF-30	DC-30	47-61	61-200
SCLF-45	DC-45	70-90	90-200
SCLF-135	DC-135	210-300	300-600

SCLF-190	DC-190	290-390	390-800
SCLF-380	DC-380	580-750	750-1800
SCLF-420	DC-420	750-920	920-2000

Price, (1-9 qty), all models: $11.45

Flat Time Delay, dc to 1870MHz



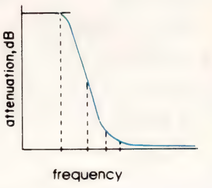
Model No.	Passband MHz loss < 1.2dB	Stopband MHz		VSWR Freq. Range, DC thru		Group Delay Variations, ns Freq. Range, DC thru		
		loss > 10dB	loss > 20dB	0.2fco X̄	0.6fco X̄	fco X̄	2fco X̄	2.67fco X̄
★BLP-39	DC-23	78-117	117	1.3:1	2.3:1	0.7	4.0	5.0
★BLP-117	DC-65	234-312	312	1.3:1	2.4:1	0.35	1.4	1.9
★BLP-156	DC-94	312-416	416	0.3:1	1.1:1	0.3	1.1	1.5
★BLP-200	DC-120	400-534	534	1.6:1	1.9:1	0.4	1.3	1.6
★BLP-300	DC-180	600-801	801	1.25:1	2.2:1	0.2	0.6	0.8
★BLP-467	DC-280	934-1246	1246	1.25:1	2.2:1	0.15	0.4	0.55
▲BLP-933	DC-560	1866-2490	2490	1.3:1	2.2:1	0.09	0.2	0.28
▲BLP-1870	DC-850	3740-6000	5000	1.45:1	2.9:1	0.05	0.1	0.15

Price, (1-9 qty), all models: plug-in $19.95, BNC $36.95, SMA $38.95, Type N $39.95

NOTE: ▲: -933 and -1870 only with connectors, at additional $2 above other connector models.

high pass, Plug-in, 27.5 to 2200MHz

HIGH PASS



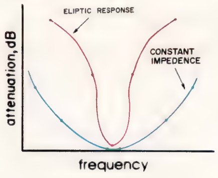
Model No.	Stopband MHz		Passband, MHz loss < 1dB	VSWR Pass-band Typ.
	loss < 40dB	loss < 20dB		
★HP-25	DC-13	13-19	27.5-200	1.8:1
★HP-50	DC-20	20-26	41-200	1.5:1
★HP-100	DC-40	40-55	90-400	1.8:1
★HP-150	DC-70	70-95	133-600	1.8:1
★HP-175	DC-70	70-105	160-800	1.5:1
★HP-200	DC-90	90-116	185-800	1.6:1
★HP-250	DC-100	100-150	225-1200	1.3:1
★HP-300	DC-145	145-170	290-1200	1.7:1

Model No.	Stopband MHz		Passband, MHz loss < 1dB	VSWR Pass-band Typ.
	loss < 40dB	loss < 20dB		
★HP-400	DC-210	210-290	395-1600	1.7:1
★HP-500	DC-280	280-365	500-1600	1.8:1
★HP-600	DC-350	350-440	600-1600	2.0:1
★HP-700	DC-400	400-520	700-1800	1.6:1
★HP-800	DC-445	445-570	780-2000	2.1:1
★HP-900	DC-520	520-660	910-2100	1.8:1
★HP-1000	DC-550	550-720	1000-2200	1.9:1

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95

bandpass, Elliptic Response, 10.7 to 70MHz

BANDPASS



Model No.	Center Freq. (MHz)	Passband I.L. 1.5 dB Max. (MHz)	3 dB Bandwidth Typ. (MHz)	Stopbands	
				I.L. > 20dB at MHz	I.L. > 35dB at MHz
★BP-10.7	10.7	9.6-11.5	8.9-12.7	7.5 & 15	0.6 & 50-1000
★BP-21.4	21.4	19.2-23.6	17.9-25.3	15.5 & 29	3.0 & 80-1000
★BP-30	30.0	27.0-33.0	25-35	22 & 40	3.2 & 99-1000
★BP-60	60.0	55.0-67.0	49.5-70.5	44 & 79	4.6 & 190-1000
★BP-70	70.0	63.0-77.0	68.0-82.0	51 & 94	6.0 & 193-1000

Price, (1-9 qty), all models: plug-in $18.95,
BNC $40.95, SMA $42.95, Type N $43.95

Constant Impedance, 21.4 to 70MHz

Model No.	Center Freq. MHz	Passband MHz loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
★IF-21.4	21.4	18-25	1.3 & 150	DC-220
★IF-30	30	25-35	1.9 & 210	DC-330
★IF-40	42	35-49	2.6 & 300	DC-400
★IF-50	50	41-58	3.1 & 350	DC-440
★IF-60	60	50-70	3.8 & 400	DC-500
★IF-70	70	58-82	4.4 & 490	DC-550

Price, (1-9 qty), all models: plug-in $14.95,
BNC $36.95, SMA $38.95, Type N $39.95

NOTE: ★**Add Prefix P, B, N, or S for Pin, BNC, N, or SMA connector requirement.**

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hardware platforms are available. The fifth tool, MATSim, which stands for Microarchitectural Timing Simulator, helps developers analyze programming timing in three modes: virtual machine mode for hardware-system design and analysis; operating-system emulation mode for developing applications; and an embedded mode. The toolkit goes for $5000. The compilers are priced at $1500 each; the architectural simulator goes for $3500; and the timing simulator starts at $4000 for two users. Tools run on IBM's RS/6000 workstations and Sun 4 platforms. *SVT*

3D DISPLAY USES POSITION SENSING, FAST GRAPHICS

Engineers at NEC Corp.'s Central Research Laboratories in Tokyo, Japan, have come up with a novel 3D graphics viewer that doesn't require special glasses or viewing screens. The system consists of very fast 3D graphics software, a sophisticated 3D position sensor, and a conventional 2D LCD screen mounted on a mechanical arm that can move in any direction. When the user moves the screen into a new orientation, the position sensor reports the new orientation to the graphics software, which calculates the new perspective of the object from the user's point of view. In addition to the basic ability to obtain a new view of the object by moving the screen, the real-time graphics software also supports zooming for closer observation, section cutting for internal views of the object, recording and playback of viewpoint-position data, and data conversion to third-party CAD software tools. NEC expects the technology to find applications in CAD-tool environments, education, entertainment, and as a presentation device. Contact Mark Pearce in Tokyo at 03-3798-6511; fax 03-3457-7249. *JS*

MOTOROLA, UNISYS COLLABORATE ON MCMS

A line of high-reliability multichip modules (MCMs) is expected from a business agreement between Motorola's Commercial Plus Technologies Operation, Phoenix, Ariz., and Unisys Corp.'s Government Systems Group, Eagan, Minn. The MCMs, designed by Motorola, will contain Motorola's processor, memory, and signal-processing ICs. Assembly will be performed by Unisys on a highly reliable thick-film-ceramic substrate technology. The modules will be targeted for harsh environments characterized by wide temperature and vibration ranges, such as those found in military and commercial avionics applications. For more information, contact Motorola's Lauren Bell at (602) 897-4867. *DM*

PLATFORM TO HELP OEMS WITH DSP-BASED PRODUCTS

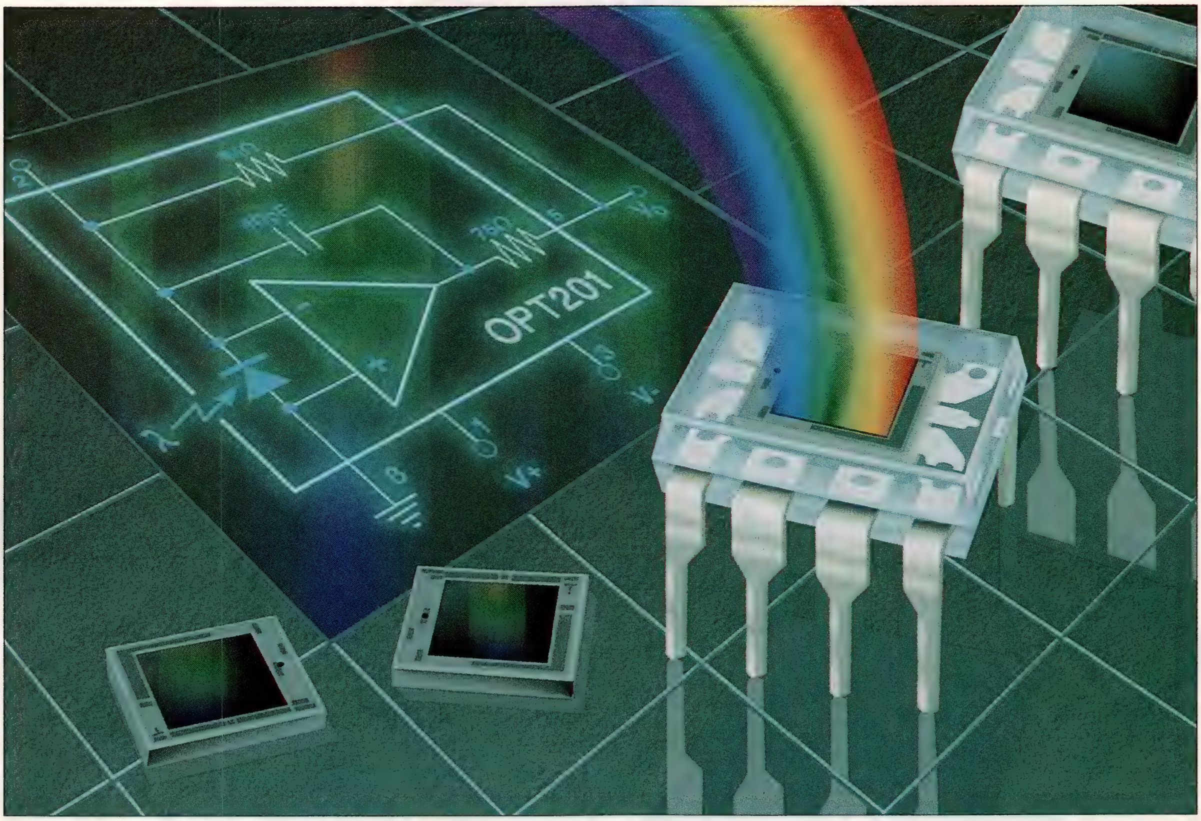
Now that IBM is offering its Mwave technology platform, OEMs will be able to bring integrated DSP-based products for PCs to market more quickly. The platform also allows OEMs to differentiate themselves at different price points by including multiple functions, such as audio processing, data communications, voice messaging, and data compression. Another feature for users is the ability to upgrade through software. For example, the transmission speed of a fax or modem can be upgraded simply by downloading software supplied by the OEM. The platform consists of DSP-based hardware and various software options that supply a link between a PC and various applications. In building an Mwave-based product, the OEMs' alternatives range from adopting IBM Microelectronics' reference designs to jointly developing a product. IBM will offer technical support, including application engineering, hardware and software development assistance, consulting services, and a toll-free telephone number. For more information, call IBM at (800) IBM-0181. *RN*

TECHNOLOGY AGREEMENT WILL PRODUCE PCI ICS

Products based on the Peripheral Component Interconnect (PCI) are expected to be the end-result of a co-development agreement between Adaptec Inc., Milpitas, Calif., and Appian Technology Inc., Sunnyvale, Calif. The two companies will jointly design and market advanced disk-interface chips based on the PCI architecture. The PCI bus offers a data-transfer rate of 133 Mbytes/s, much higher than the conventional ISA bus supplies. The agreement calls for both Adaptec and Appian Technology to develop high-performance PCI-to-Integrated Device Electronics (IDE) disk-interface ICs for PC motherboards and add-in cards. The interface chips can transfer 50 Mbytes/s, a significant increase over standard IDE components, which usually are hard-disk drives. Products based on the PCI-to-IDE interface should be announced by the two companies shortly. For additional information, contact Adaptec at (408) 945-8600, or Appian Technology at (408) 730-5477. *RN*

New

Photodiode & Amplifier IC Simplifies Designs



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uts Discrete Designs In The Dark

PT201's unique combination of photodiode and amplifier eliminates any problems commonly associated with discrete designs such as eakage-current errors, noise pick-up, and gain peaking due to stray apacitance. Available in a transparent mini-DIP, it's light years ahead f the competition.

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• Supply range	±2.25V to ±18V
• Quiescent current	400µA
• Packages	transparent mini-DIP, dice

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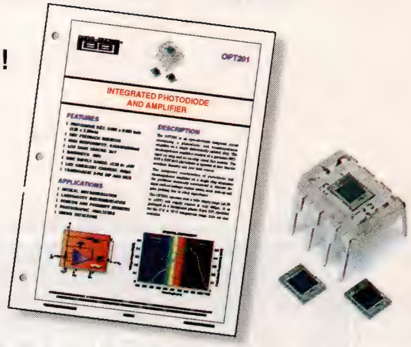
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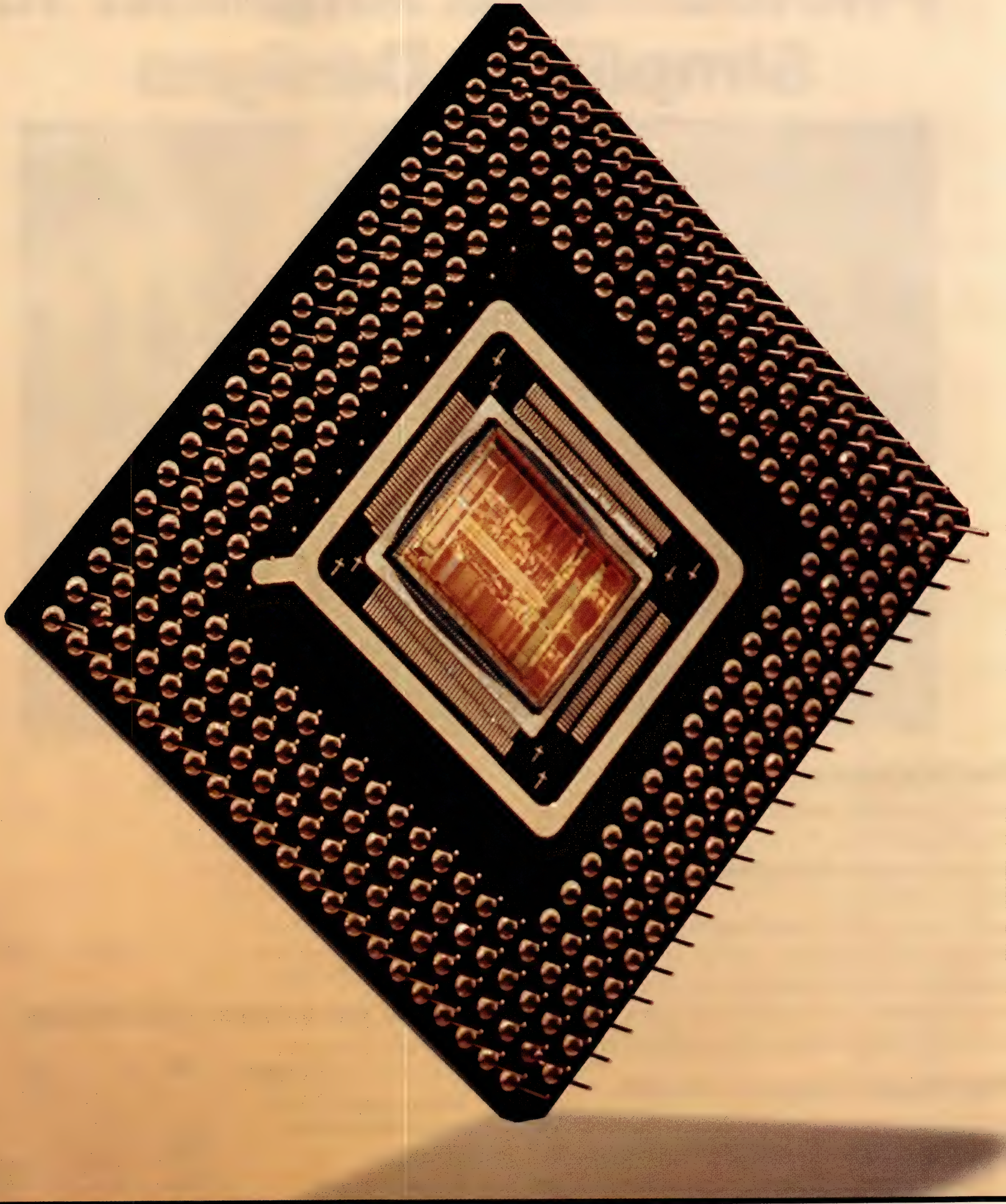

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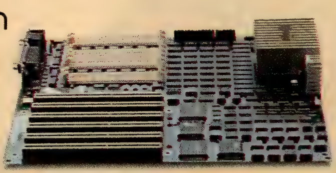

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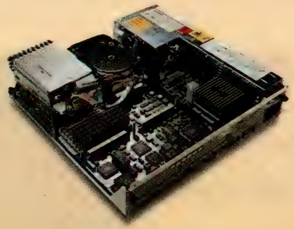

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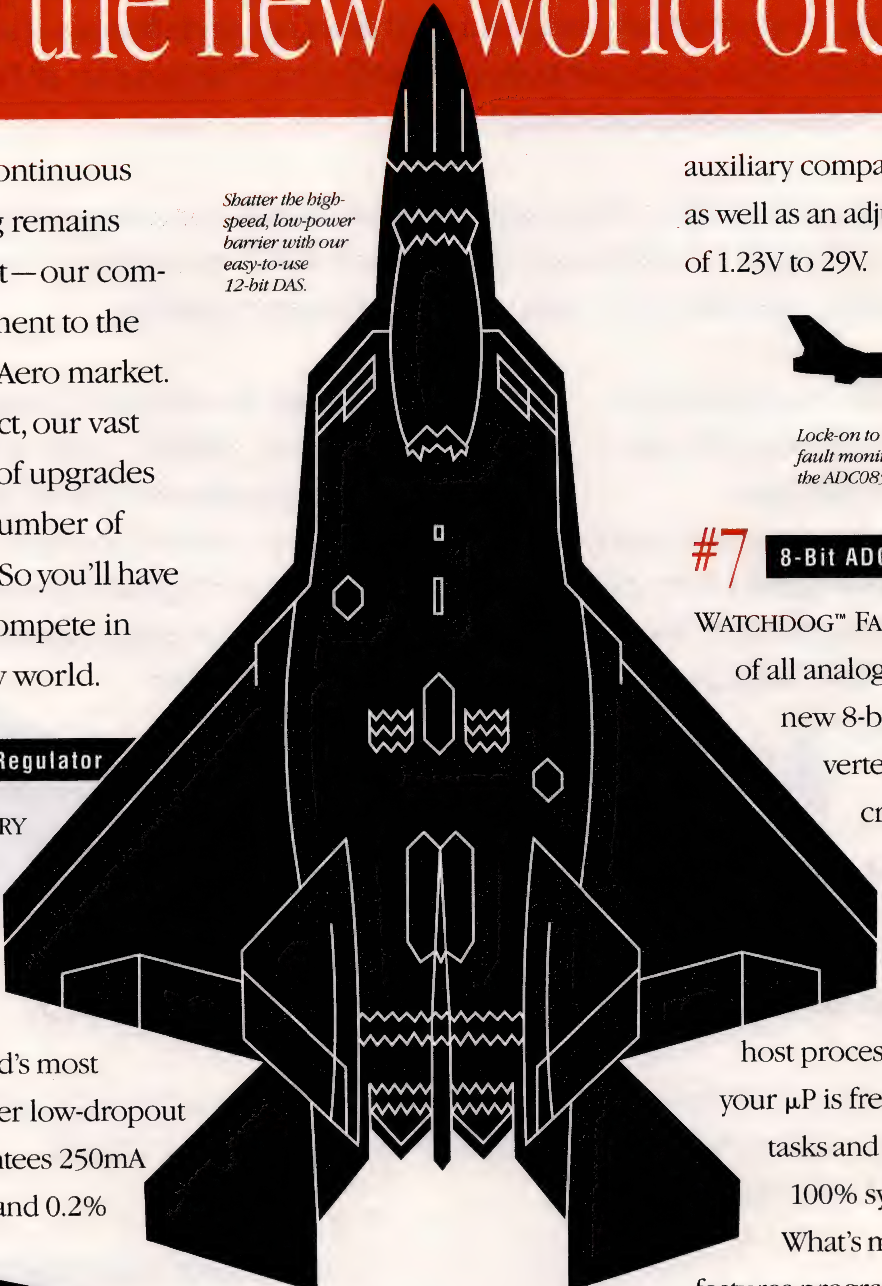

Shatter the high-speed, low-power barrier with our easy-to-use 12-bit DAS.

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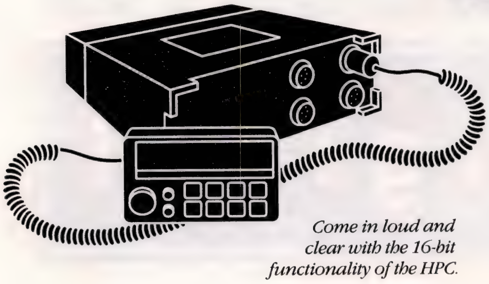
In this world of continuous change, one thing remains constant—our commitment to the Mil/Aero market. In fact, our vast arsenal of upgrades now includes a number of new innovations. So you'll have what it takes to compete in today's brave new world.

#1 **Low-Dropout Regulator**

GET LONGER BATTERY LIFE with ultralow dropout (<470mV) and quiescent current. The LP2953 is the world's most precise micropower low-dropout regulator. It guarantees 250mA of output current and 0.2% load and line regulation over the full military temperature range, which reduces your total error budget and external components. Plus, it also has shutdown and auxiliary comparator functions as well as an adjustable output of 1.23V to 29V.



Come in loud and clear with the 16-bit functionality of the HPC.

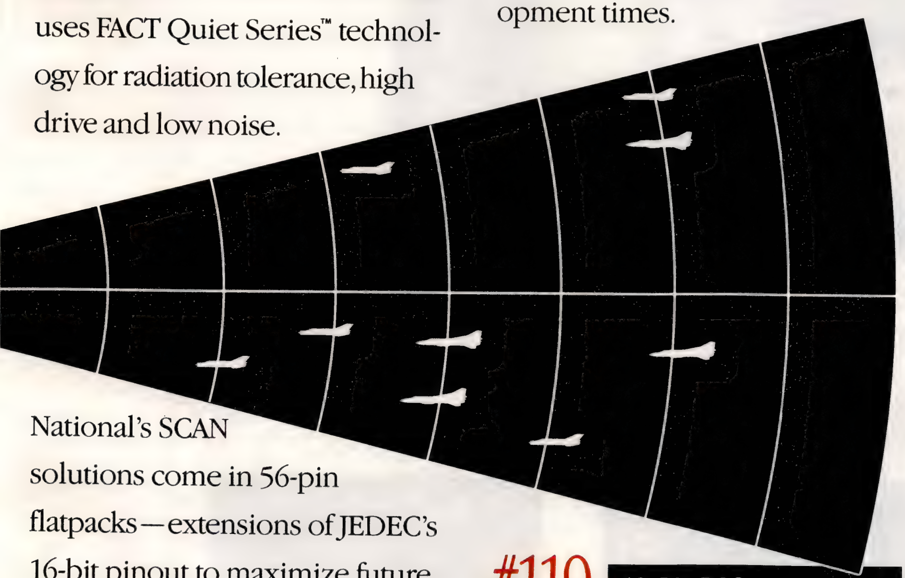
Lock-on to "watchdog" fault monitoring with the ADC0858.

#7 **8-Bit ADC**

WATCHDOG™ FAULT MONITORING of all analog functions. Our new 8-bit A-to-D converter delivers flight-critical monitoring of temperature, voltage and current independently of its host processor. As a result, your μP is free to do other vital tasks and you're guaranteed 100% system operation. What's more, the ADC0858 features programmable limits, an on-board MUX, eight analog inputs, +5V single-supply operation and a mere 50mW power budget.

#37 SCAN Solutions (1149.1)

BOUNDARY SCAN TESTING made easy. Our family of 18-bit SCAN™ (Serially Controlled Access Network) solutions are fully compliant to IEEE 1149.1. It's a highly integrated, low-power family that uses FACT Quiet Series™ technology for radiation tolerance, high drive and low noise.

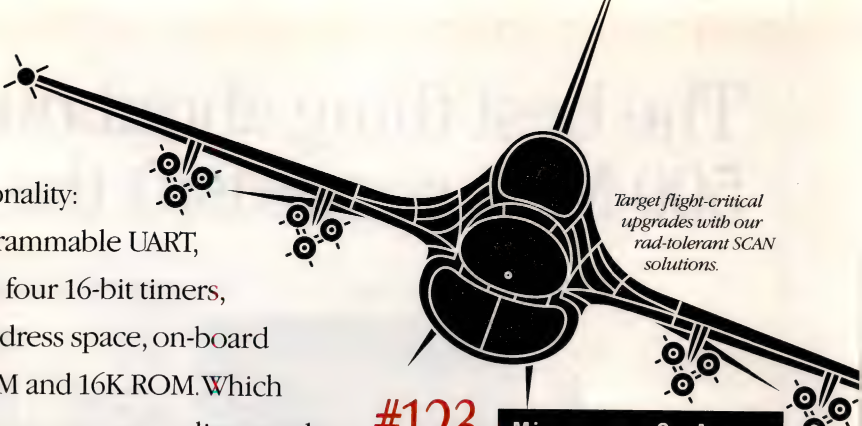


National's SCAN solutions come in 56-pin flatpacks—extensions of JEDEC's 16-bit pinout to maximize future upgrade flexibility.

#101 16-Bit Microcontroller

FULL 16-BIT FUNCTIONALITY in a data-moving machine. When it comes to speed-critical signal processing, no other µC whips through data faster on less code than our 16-bit HPC. And nothing delivers so much full-featured functionality: a programmable UART, at least four 16-bit timers, 64K address space, on-board 512 RAM and 16K ROM. Which means now you can realize greatly reduced system costs and development times.

Upgrade your takeoffs with the micropower precision of the LM6061.



Target flight-critical upgrades with our rad-tolerant SCAN solutions.

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EASY-TO-USE 12-bit Data Acquisition System. Our monolithic LM12H458 is not only the fastest 12-bit plus sign DAS around, it's also the easiest-to-use. And that's just for starters. This software-programmable 140KS/s and 34mW (max @ 5V) performer is also unequaled in integration, sporting such on-board features as a MUX, FIFO, timer, instruction register, reference and S/H. All of which adds up to increased performance and enhanced reliability.

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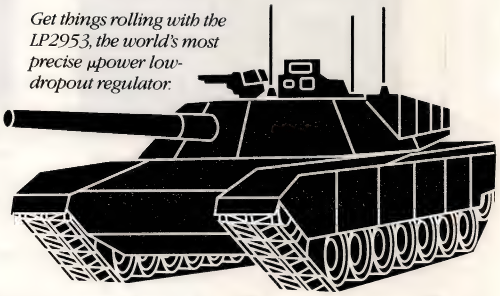

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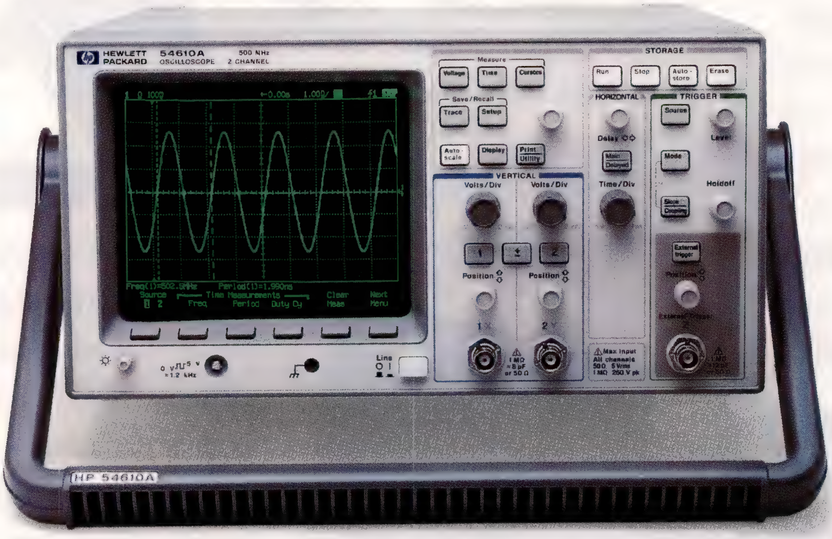
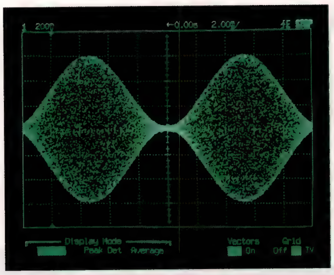
The best thing about our 500 MHz scope isn't the low price.



It's what you get for it.



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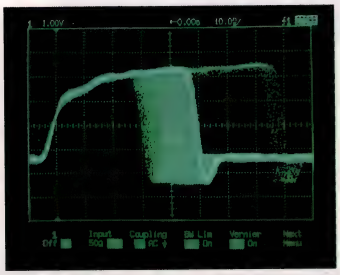

A bright trace and convenient, push-button functions like Autostore let you easily see and store tough-to-find signals.

Pretrigger viewing and delayed sweep mode help you save time by grabbing and displaying signals before or after the trigger event.

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How we can offer you a 500 MHz, delayed sweep scope that's within budget, without compromise.

High bandwidth digital scopes have always forced you to sacrifice two things you love about analog scopes: a familiar look and feel and immediate, believable displays.

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Call HP to see how much scope you can get for your money.

Discover just how easy it is to afford a high bandwidth, high accuracy oscilloscope by calling your local HP sales office or one of the numbers listed below. Once you hear the price, we think you'll agree it's the best deal of any 500 MHz scope.

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CLEANING SCHEME MAKES CONTAMINANTS GO AWAY FOR A WIDE RANGE OF MATERIALS

A novel cleaning process has been developed to remove particles and even fingerprints from silicon, gallium arsenide, aluminum, and many other materials. Employing a non-reactive gas-phase system, the process is environmentally benign since it uses no water or reactive chemicals. Tests conducted thus far show the process removes surface organic films, inorganic films, and particles as large as 5 μm to as small as molecules. The process was developed by Radiance Services Co., Bethesda, Md.

Cleanliness is one of the key factors driving up the cost of new semiconductor manufacturing facilities. With sub-micron feature sizes on advanced manufacturing processes, particles as small as 0.1 μm could be damaging. For instance, Intel estimates that on its most advanced microprocessor technology, one "killer" particle drives the cost of its billion-dollar fabrication facility up by $8 million. If the number of such particles reaches 150 per wafer, the projected increase in facility capital costs close to double the facility construction cost. Thus, the need arises for a low-cost, environmentally benign cleaning approach that removes all particles and contaminants.

The new process combines deep ultraviolet light available from a krypton-fluoride (KrF) excimer laser or a bulb and a flowing inert gas, a combination that keeps overhead costs low and is very easy to implement *(see the figure)*. The deep ultraviolet photons break the contaminant-surface bonds and levitate the contaminant from the surface. The contaminant is then entrained in a flowing inert gas such as nitrogen or argon, and the gas can be scrubbed and reprocessed for reuse, thus minimizing the waste produced by the system.

Minimal surface damage also results from the cleansing technique—a microroughening of less than 1 Å—and it can remove metallic ions as well as all the other materials mentioned. Furthermore, the company recently demonstrated the removal of particles as large as 80 μm.

The scheme can also remove contaminants that current wet-processing methods cannot remove. And it can do so without expensive support such as deionization water plants, waste-treatment plants, and waste-disposal sites.

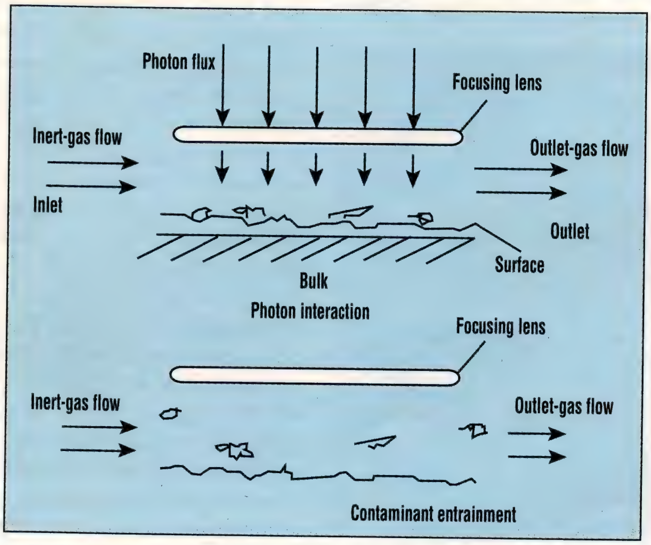
The process can be adapted to either cluster or stand-alone tool configurations. In stand-alone configurations, it can clean about 400 wafers/day at a projected cost of less than $2 per wafer. In comparison, wet cleaning costs about $7 per wafer.

A cluster module for vapor-phase hydrogen-fluoride (HF) gas is in development. A potential limitation, though, is the requirement for rigorous control of the HF vapor to prevent microroughening of the material surface. The microroughening on a chip's surface can cause device performance degradation and thus overall circuit degradation or failure.

The new cleaning system can tackle large-scale contamination, such as that found in aerospace, medical, optical, and automotive industries. Although the company developed the process, it does not sell cleaning systems but it does sell licensing arrangements that tie royalties into the added productivity.

For more information, contact Donna Fitzpatrick at (301) 654-0228.

DAVE BURSKY

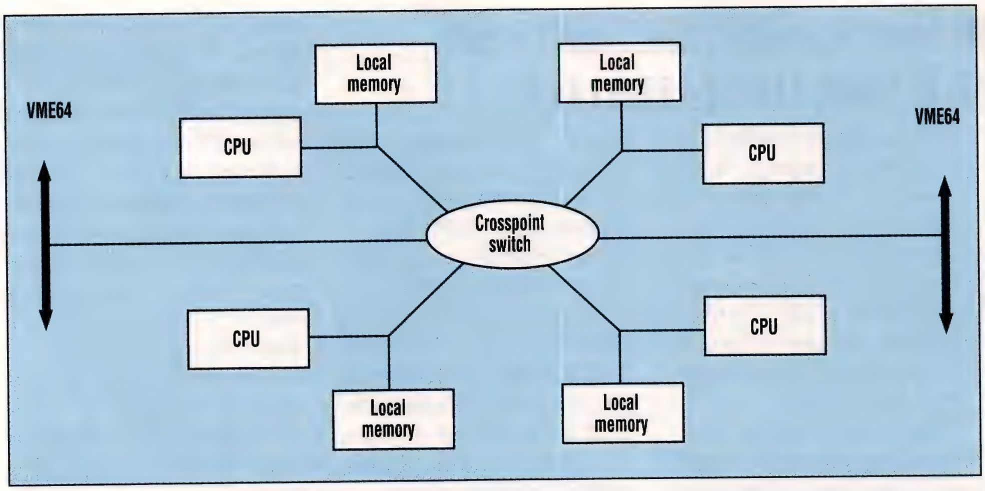


CROSSPOINT-SWITCH BOOSTS MULTIPROCESSOR PERFORMANCE

It's well known that multiprocessor systems can process more information than uniprocessor systems. But having two processors doesn't necessarily double the processing power of a uniprocessor system. That's because there's some overhead associated with the additional processors, specifically in the communications between processors and memory, that limits the amount of information that can be passed between CPUs. As successive processors are added, performance gains become smaller and smaller, eventually reaching a point where adding another processor provides virtually no gain.

Using a crosspoint switch architecture, designers at Concurrent Computer Corp., Oceanport, N.J., may have a solution. They developed an architecture that can increase performance linearly, with a 95% boost with each added processor. The system is currently limited to four processors. The architecture will appear in the company's Maxion multiprocessor system, which should debut in January.

The company calls its architecture UltraSmart, for scalable multiprocessor architecture for real time. It consists of three components: a crosspoint processing unit and memory module, a crosspoint I/O module, and an I/O-conditioning module. An auxilia-



ry VME module is available for expansion.

One crosspoint processing unit is needed for each CPU in the system. The module contains the CPU (a 150-MHz MIPS RISC R4400), a 1-Mbyte write-back secondary cache, a cache-coherency directory for cache-memory management and a memory subsystem that supports 16 to 128 Mbytes.

The crosspoint switch, housed in an ASIC, serves as the key component in the architecture. It supports multiple independent point-to-point connections between six independent ports. Each port can transfer 400 Mbytes/s, for a maximum system bandwidth of 1.2 Gbytes/s. Four ports are connected to the four independent CPUs (each configured with local memory); one port is connected to the I/O adapter; and the remaining port can be connected to a VME adapter or reserved for future expansion. Note that the local memory of each CPU can be accessed by any of the other CPUs *(see the figure)*.

In the crosspoint architecture, cache memory is managed using a cache-coherency directory. The directory is implemented as a 7-bit tag-word with every 32-bit cache line. One of the seven bits is reserved as the cache dirty bit and the remaining six bits correspond to the six switch ports. With each memory access, the tag word is examined. If one of the six bits is set, a message is sent to the switch that invalidates the cache associated with that particular port. This technique is similar to traditional bus snooping, except that overhead only occurs when the cache bits change state.

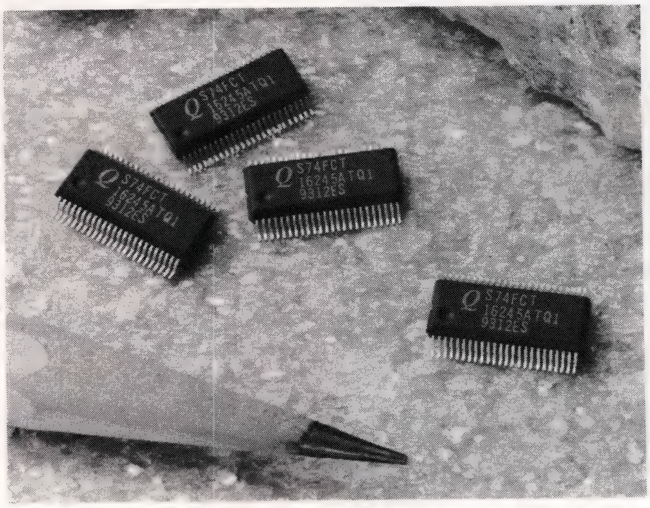
For more information, contact Concurrent Computer at (908) 870-4500.

RICHARD NASS

TINY SMT PACKAGE SHRINKS BUS-LOGIC DEVICES

The miniaturization merry-go-round that eventually finds its way to all system components has once again stopped off at bus-interface circuitry. The quarter-size-outline package (QSOP), developed in 1990 by Quality Semiconductor Inc. (QSI), Santa Clara, Calif., was touted at the time as the most space-efficient surface-mount package ever for 20- and 24-pin FCT logic devices. Now the company has tightened the package's pin pitch and metamorphosed it into a highly efficient vehicle for double- and triple-width logic functions.

The QVSOP package offers an outline of just 150 by 390 mils and a pin spacing of 15.7 mils (0.4 mm). This is identical to the lead spacing used on many high-pin-count plastic quad flat packs. For its part, the package outline is the same as that of standard 14-pin SOICs *(see the photo)*. But at a 15.7-mil lead pitch, the QVSOP carries 48 leads, which enables it to hold more than one byte-wide logic device and still have extra pins left over for multiple ground connections.

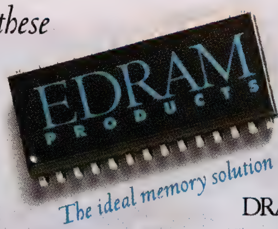


According to Mike Davis, product marketing manager at QSI, the QVSOP's development parallels that of the QSOP, which leveraged the large existing test, handling, and assembly infrastructure surrounding the SOIC by retaining its 150-mil width. Similarly, the QVSOP maintains the body width of the QSOP and takes density further by virtue of a shrinking pin pitch.

The solution for double- and triple-width logic presented by the QVSOP solves the potential dilemma of having to design and fabricate a 16-bit-wide logic device in silicon. There's a tradeoff between the lower sort yields a larger die would bring and the higher integration it offers, and the QVSOP neatly sidesteps that issue. The only real benefit of the silicon-integration approach, Davis says, is skew control. But because the multiple die in a double- or triple-width QVSOP package come from the same wafer

Trying to unravel the issues of high memory bandwidth?

EDRAM can solve these knotty problems.



With bus rates going higher and higher, the traditional approaches of interleaving or combining DRAM with cache just add more complexity to your system... without really solving the performance problems.

The best solution is Ramtron's family of Enhanced DRAMs (EDRAMs). They provide 15ns page reads and writes. There's no page-miss penalty either. You get better random read/write performance than interleaving, cache or even SDRAMs.

In short, EDRAMs deliver performance with big savings, less space, lower power and no complex controllers for interleaving or caching. They're the first practical solution for high-bandwidth designs. And compatibility with today's DRAMs allows a simple upgrade path.

Don't get tied up with yesterday's memory approaches. Get all the details by calling 1-800-545-DRAM, Ext. AE05 today.

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DM2200	4Mb x 1	15ns	35ns/15ns	300 mil SOJ
DM2202	1Mb x 4	15ns	35ns/15ns	300 mil SOJ
DM2212	1Mb x 4	15ns	35ns/15ns	300 mil SOJ
DM1M32, 36	1Mb x 32,36	15ns	35ns/15ns	72 pin SIMM
DM2M32, 36	2Mb x 32,36	15ns	35ns/15ns	72 pin SIMM

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lot, and the package's leadframe inductance is carefully controlled, skew isn't much of an issue anyway.

Another advantage in the multiple-die-per-package technique is that QSI can take any available logic device, including its QuickSwitch devices, and place them in the QVSOP in any combination. A register and a QuickSwitch combination could serve as a bypassable register block or function.

The technique also enables QSI to incorporate series-termination resistors within the logic devices. Such resistors are typically placed in line with the data bus to reduce the slew rate and, therefore, reduce ground bounce, ringing, and reflection. Placing the devices on silicon within the logic-device package can often make a considerable difference in the circuit's function in terms of noise.

JEDEC approval was already bestowed upon the QVSOP, making it a recognized industry standard for SMT logic packaging. As far as packaging directions go for future generations of 32- and 64-bit-wide logic, QSI plans to simply extend the QVSOP lengthwise and add more pins at the same 0.4-mm pitch.

"When you think about packaging for a 32-bit die, there'll be 32 pins worth of input, 32 pins worth of output, and then power, ground, and control pins," Davis muses. "You're probably talking about a 100-pin package." Though today's 100-pin packages are for the most part square plastic QFPs, Davis believes space savings are diminished in going to a larger but square package because both the package's total area would be greater than the QVSOP's if it were simply made longer to accommodate the extra pins.

DAVID MALINIAK

HIGHLY INTEGRATED 386-CLASS CPU LETS USERS FLEX INDIVIDUALITY

The surging interest of late in intelligent portable digital systems seems to center on the availability of high-performance, low-power, and highly integrated central processing units.

For instance, specialized RISC (reduced-instruction-set computer) processors are starting to appear for personal digital assistants (PDAs). However, the broad industry experience with the x86 instruction set and architecture, as well as the availability of low-power 386 central processing units targeted at laptop computers, has fostered a demand for highly integrated 386-compatible processors.

When integrating features onto the processor,

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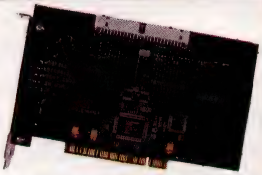

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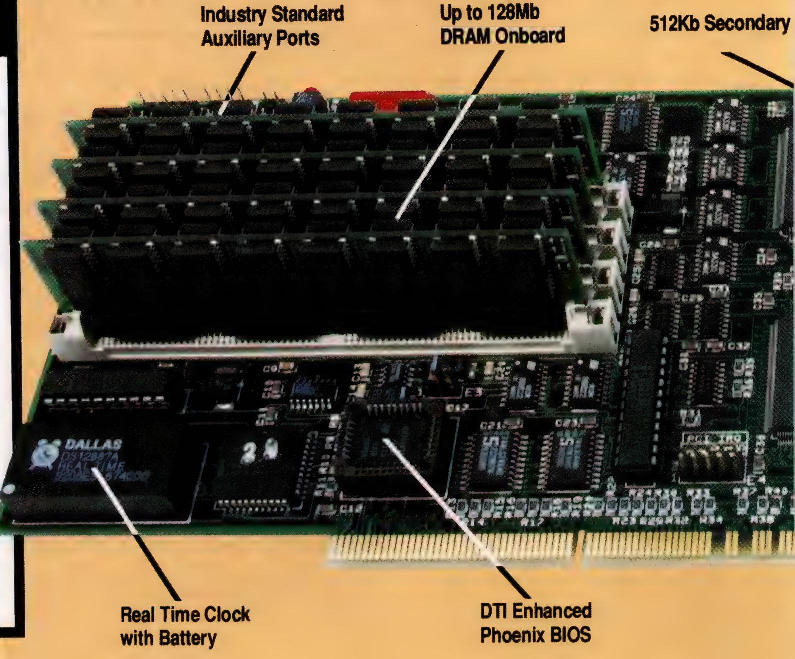
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DTI Enhanced Phoenix BIOS

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most designers will find that no two applications require the same exact feature set.

By basing its high-integration CPU developments around a standard-cell library and its Am386SXLV processor core, the designers at Advanced Micro Devices Inc., Austin, Texas, were able to come up with a malleable, highly integrated, 386-compatible processor.

The AMD processor can be "tuned" by the customer just by adding new functions or removing unwanted ones.

Code-named ELAN, the 386-compatible processor is formed from fully-static CMOS logic. The core CPU can operate at supply voltages down to 3.3 V, while the I/O pads run at either 3.3 or 5 V.

To minimize system power consumption and maximize operating time when running from batteries, the designers of the CPU also included power-management logic on the processor chip.

In addition to this development, a system-management mode (SMM) was also included to allow for background execution of power-management routines, or to make possible other housekeeping operations.

The first version of the ELAN chip, released by Advanced Micro devices just last month, possesses a well-rounded set of features targeted at PDA-type applications. These features include a pair of PCMCIA 2.0 card slots; serial- and parallel-port interfaces; interrupt, DMA, ISA-bus, and LCD panel controllers; counter-timers; and a real-time clock.

Those resources also suit the chip to other applications, including medical or industrial instruments and specialized data-collection devices.

To make the ELAN chip flexible, the company's designers created a flexible on-chip clock generator that is based upon a phase-locked loop. The clock generator requires just an off-chip crystal. It also provides all of the timing signals for both on-chip and off-chip functions. Moreover, it can be programmed to run at many different rates. With five programmable output pins, the power-management logic can control off-chip system functions for additional system flexibility.

The flexible clock generator, coupled with the power-management logic, gives the designer five operating modes. Each mode provides progressively more power savings as the chip descends into its lowest power states.

Unlike other 386-compatible CPUs, the ELAN processor incorporates an LCD controller that can handle displays with resolutions of up to 640 by 400 pixels. In addition, the local-bus interface on the processor allows the designer to tie in a video controller when an LCD panel isn't sufficient.

For more information, contact Gary Baum at (512) 462-5459.

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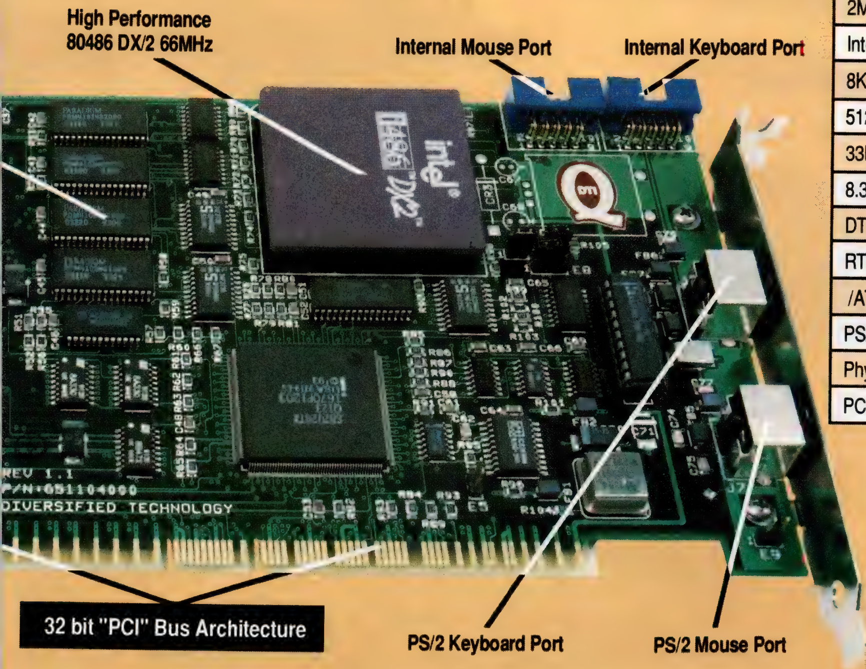

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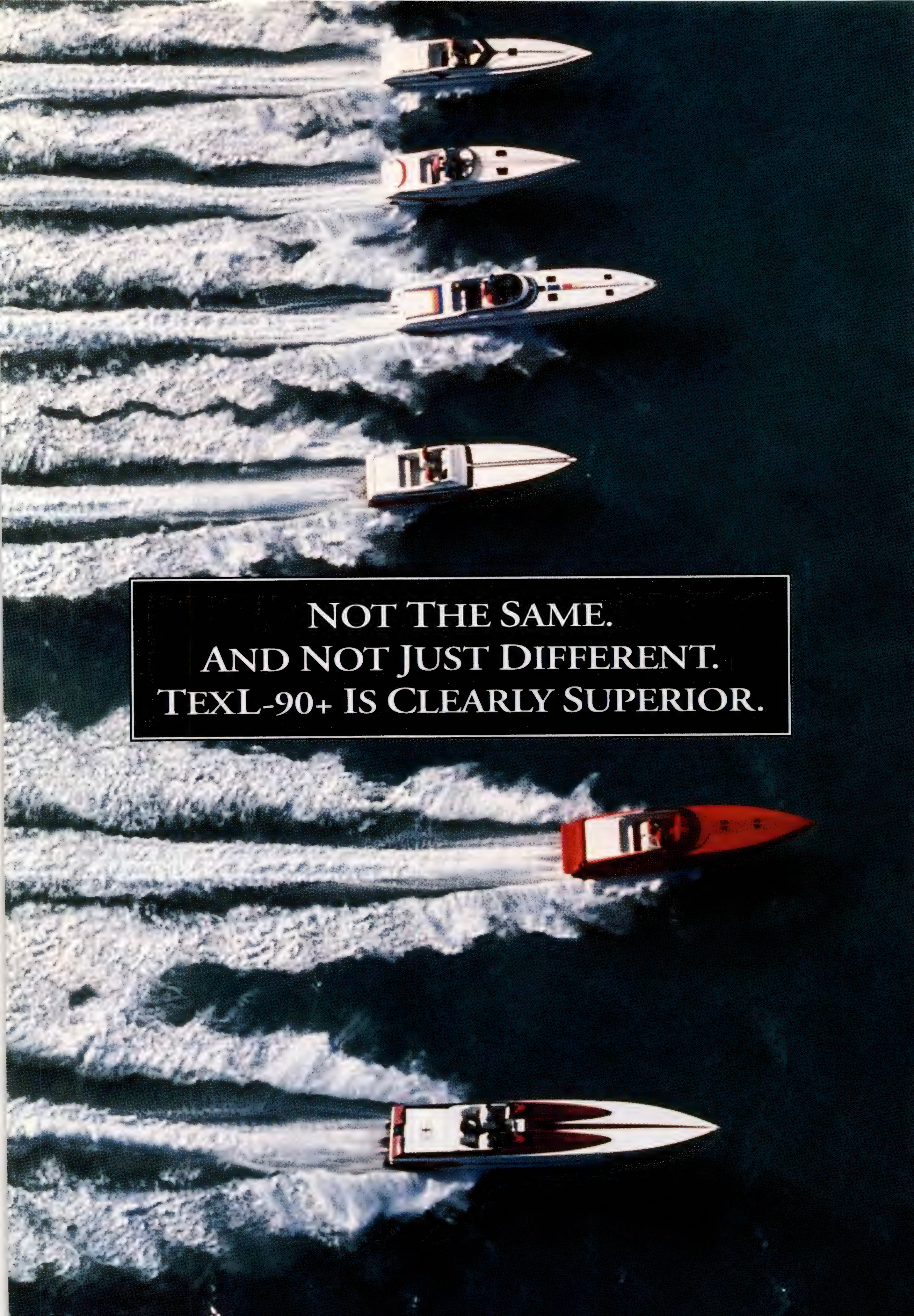
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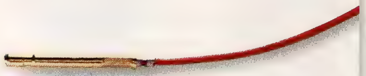

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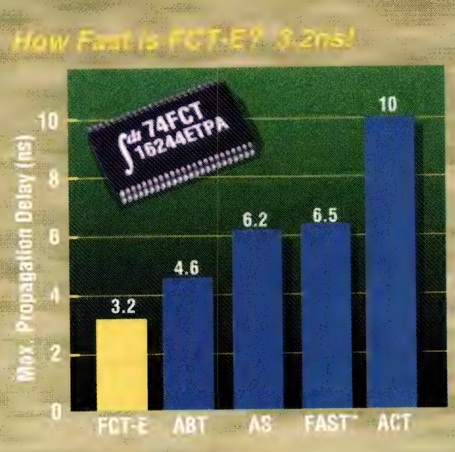

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MULTIMEDIA AND PCMCIA HIGHLIGHT FALL COMDEX

DIGITAL AUDIO AND VIDEO LIVEN UP THE TRADE SHOW FLOOR, WHILE PCMCIA ADVANCES MAKE IT PORTABLE.

RICHARD NASS

Applications such as multimedia and video teleconferencing were only a twinkle in the eye of system designers as recently as two years ago. Now, with the advances in digital audio, video, and DSP technologies, such applications are coming to fruition. In fact, they'll be lighting up the displays and enhancing the speakers at Fall Comdex, to be held in Las Vegas from Nov. 15-19. Also on tap at the show are the latest PCMCIA efforts for the portable office.

In digital-video applications, overlay and in-laid video devices are the two main approaches taken by designers. Overlay products, which are the more common of the two, use dual frame buffers and are traditionally designed for viewing video. In-laid designs suit video capturing and employ just one frame buffer. Although a move toward more in-laid solutions is progressing, mainly due to economic reasons, in-laid techniques require greater integration of video-scaling capabilities.

A board developed by Orchid Technology, Fremont, Calif., which will debut at Comdex, combines the benefits of both approaches. In addition to capturing and viewing video, it can scale images. For example, if a very small video window is captured, it can be played in a much larger window (at the same resolution) without any loss in quality. As a result, users are able to store larger video clips and not sacrifice any extra disk space.

"The bulk of the technology today offers small grainy postage-stamp-size video windows. This low quality of current-generation products is turning some users off," says Jon Siann, product manager for multimedia systems at Brooktree Corp., San Diego, Calif. "But, as we've seen with sound, when you deliver high quality, it becomes very attractive to users."

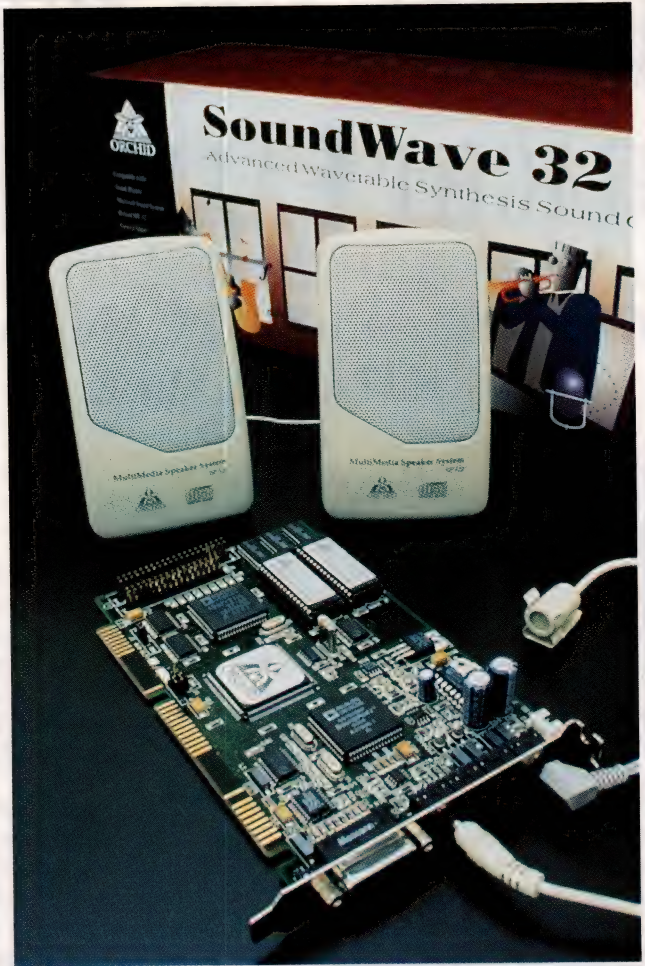
INTEGRATION IS KEY

Brooktree sees integration as part of the OEMs' performance hurdle that must be overcome. Says Siann, "The technology is there from multiple vendors, but it's not packaged correctly. An OEM building a truly multimedia box needs to go to four or five different vendors to build the complete system. That bumps up the system costs, partly because these devices weren't designed to work together—they were designed in a vacuum. It also creates redundancy in components, causing the OEM to pay for more functionality than is needed. In addition, OEMs ask 'how do you make all the chips work together, who will write the software, and what happens if there's a compatibility problem?' Many PC OEMs don't have the resources to handle these issues."

Brooktree will demonstrate its Hammerhead board at Comdex. The company is calling it a complete turnkey design, meaning that everything an OEM needs to manufacture a board is at hand, including all of the hardware and software. The board, built with a video-cache technology, supplies full-screen, high-quality video at 30 frames/s using a software codec. The video cache employs a shared frame buffer for both video and graphics.

Another issue confronting the digital video environment is interface selection. Some of the interface standards being proposed are the VESA Advanced Feature Connector (VAFC); the VESA Media Channel (VM-Channel) *(see "Looking beyond the VAFC," p. 115)*; the SFBI (shared frame-buffer interface) from Intel and ATI Technologies; and PCI, also developed by Intel.

A silicon solution devised by AuraVision, Fremont, Calif., is suited for a host of video applications, including capture, display, editing, conferencing, and multimedia. Its VxP500 video record and playback processor employs cost-effective DRAM as a single, continuous-frame buffer, rather than a more expensive video RAM architecture. Using built-in compression algorithms, 30-frame/s video can be captured without any loss of quality.


SoundWave 32
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1. SPEAKERS AND A MICROPHONE accompany the SoundWave 32 audio board devised by Orchid Technology. It employs an Analog Devices ADSP2115 DSP chip to combine multiple sound standards and play them simultaneously. The board comes with over 8 Mbits of on-board sound samples.

The VxP500 uses an internal cache memory to get around the bandwidth problem that typically hinders multimedia systems. This architecture helps to accelerate the video playback. Using acceleration, it's easier to keep the audio and video synchronized during playback without dropping any motion video frames, even when utilizing a full screen. The chip, which is operating-system independent, supports 16.7 million colors at 24 bits.

AuraVision offers a developers kit that includes an evaluation board, schematics, device drivers, and debuggers. In large quantities, a complete VxP500-based board, with memory, should cost about $100.

Rambus Inc., Mountain View, Calif., came up with a DRAM architecture for displaying digital video because it can reduce the host system's latency. The architecture can pass 500 Mbytes/s across a 9-bit-wide channel to remove the bottleneck that exists between the host processor and the system's main memory. The company's 4-Mbit part, called RDRAM, built with a standard 0.8-µm CMOS process, operates at 500 MHz. An 18-Mbit 0.5-µm part is in the works. The current chips, manufactured for Rambus by Toshiba, offer a very low pin count (32 pins), while requiring less chips than a conventional DRAM solution. Because fewer parts are needed, the memory draws less power. This, combined with the lower parts count, makes the architecture suitable for portables as well as desktops.

Comdex isn't solely a visual show, though, as sound-board introductions will be plentiful. One example comes from Orchid Technology, which developed the SoundWave 32 board, speaker, and microphone package *(Fig. 1)*. The board takes advantage of DSP technology to support and combine a host of sound and multimedia standards, including AdLib, MIDI, SoundBlaster, and Windows Sound System. This means that, for example, it can emulate the 16-bit audio of the Windows Sound System while simultaneously supporting MIDI wave synthesis and SoundBlaster specifications.

SOUNDING OFF

The SoundWave 32 is based on an Analog Devices ADSP2115 DSP chip that's capable of processing 20 MIPS, more than ample horsepower to perform the wave-table and FM synthesis required to produce the sounds. The board comes with over 8 Mbits of on-board sound samples. Also, 16-bit stereo audio and adaptive-differential, pulse-code modulation (ADPCM) compression let users store the sounds directly on the host's hard-disk drive without taking up lots of disk space.

In addition to the wave-table and FM synthesis methods of creating sounds, there's another technique that's currently on the drawing board—waveguide synthesis. Waveguide synthesis, developed by researchers at Stanford University, doesn't sample an entire sound like wave-table synthesis. It actually defines a complex equation to represent each sound. Then the sound can be altered by plugging different variables into the equation. Furthermore, with wave-table synthesis, all of the acoustic waveforms must be stored in ROM, which can consume a fair amount of memory space. Conversely, waveguide synthesis only stores a table of parameters for each equation.

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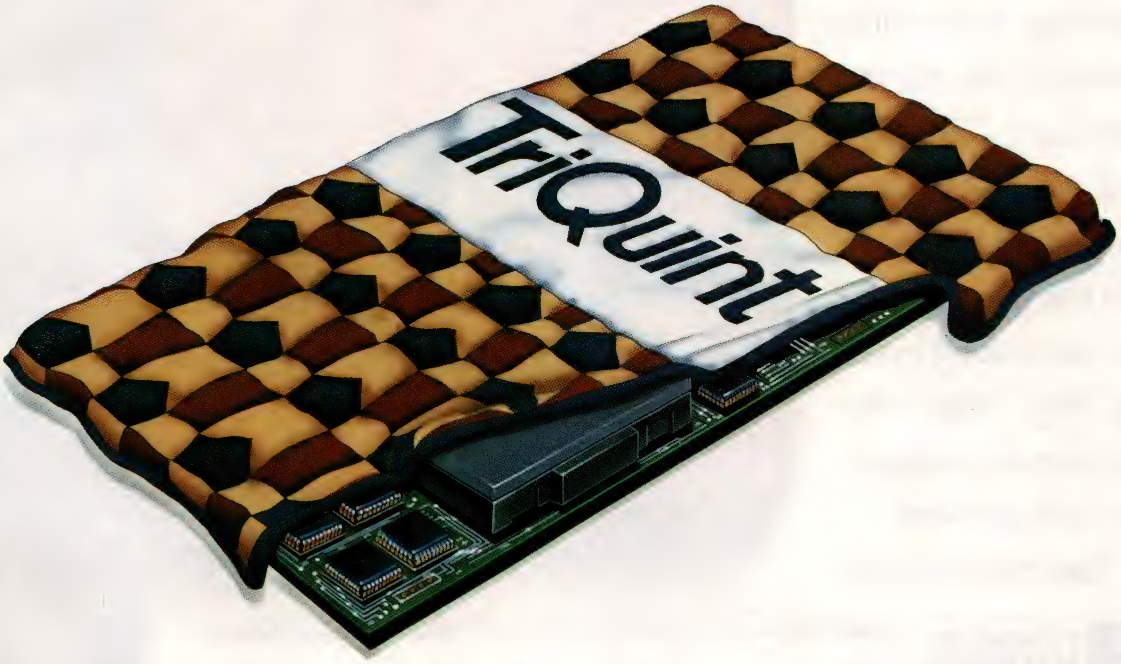

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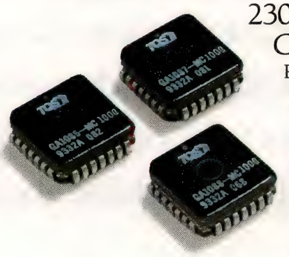

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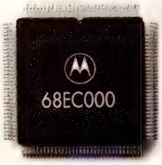

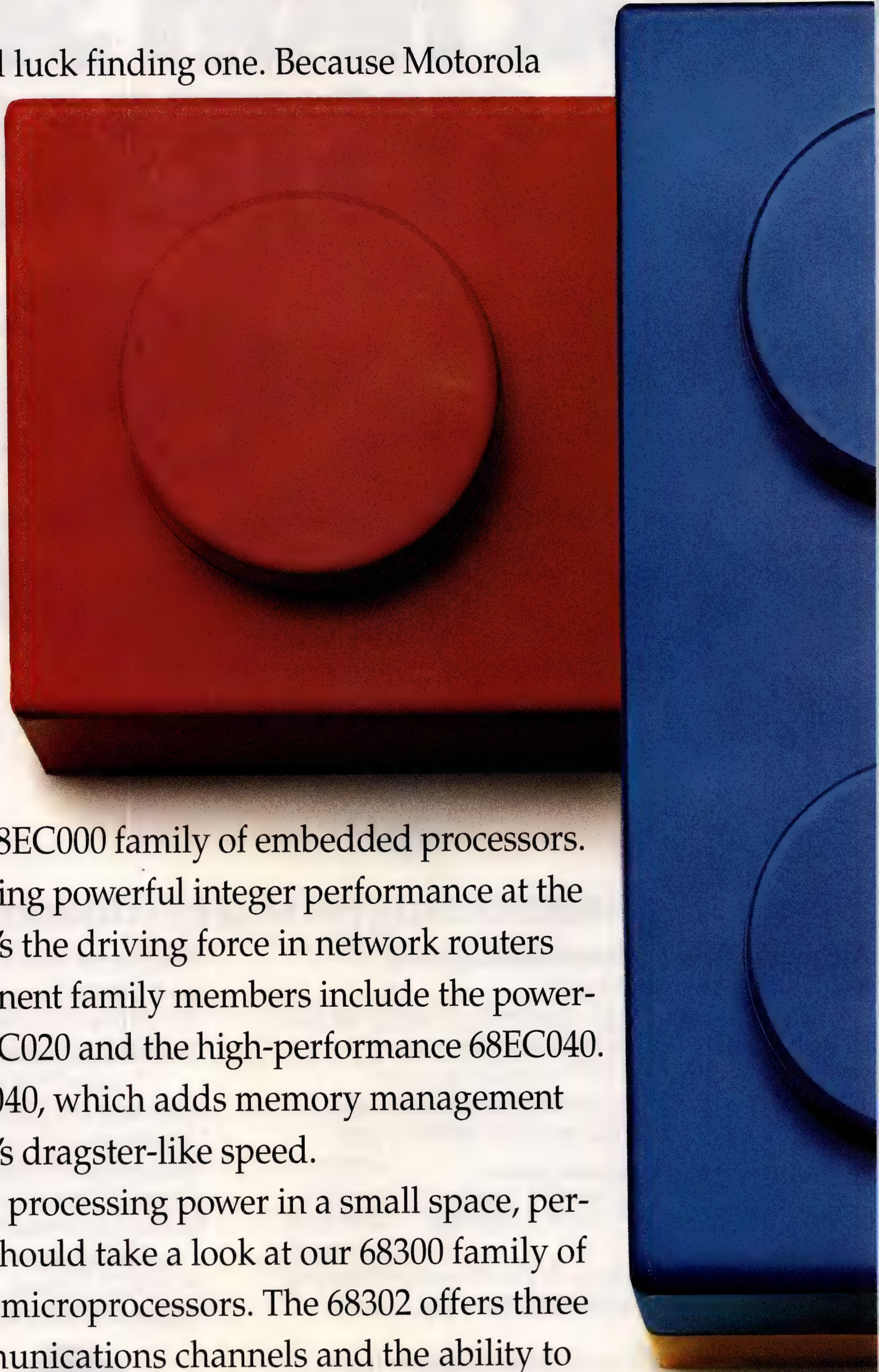

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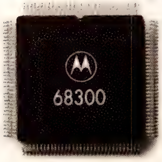

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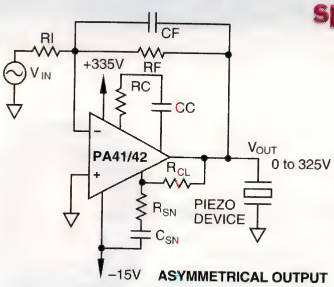

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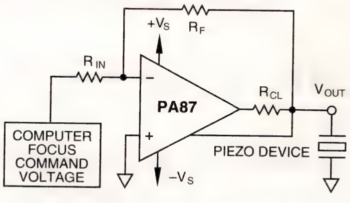

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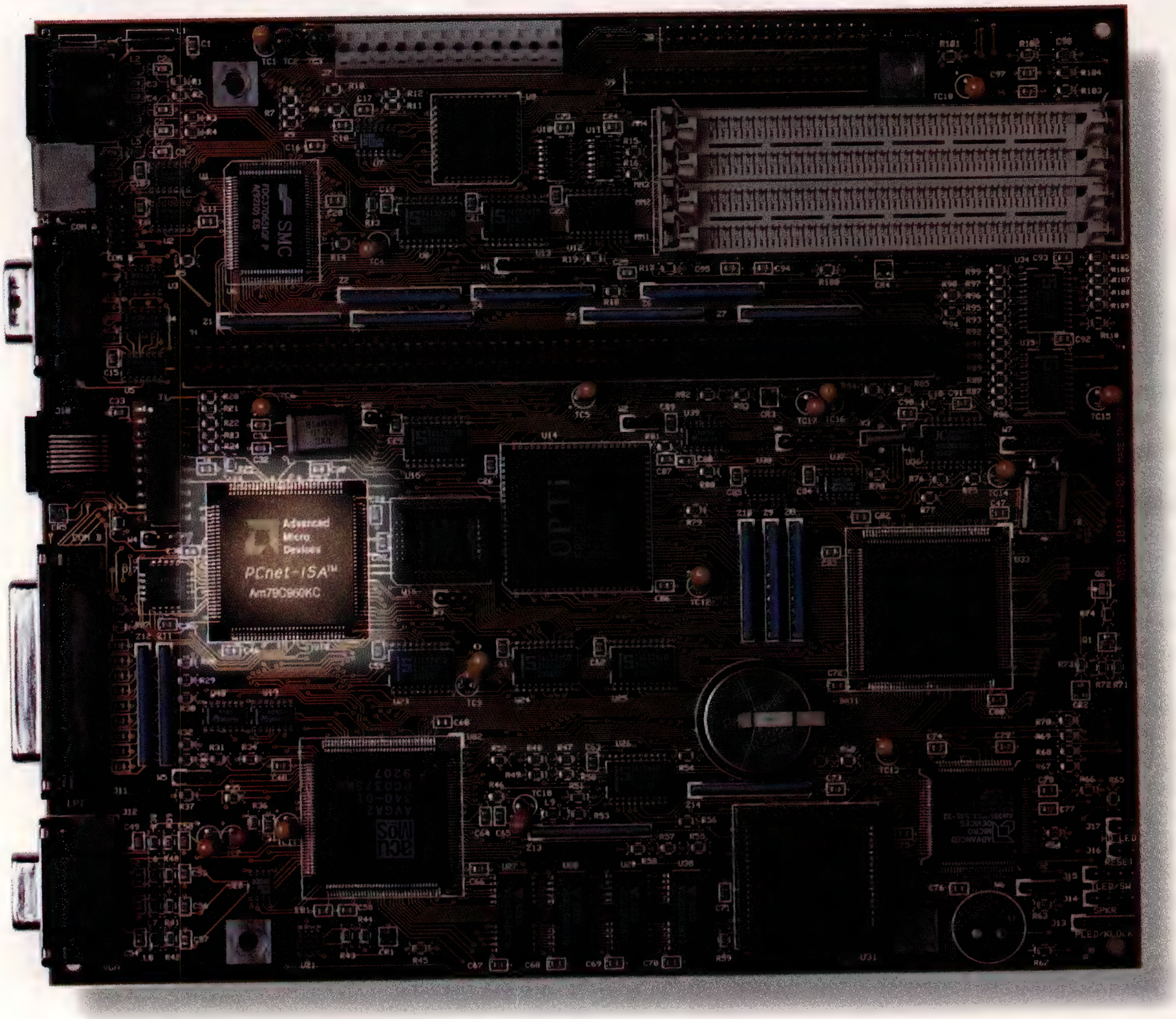

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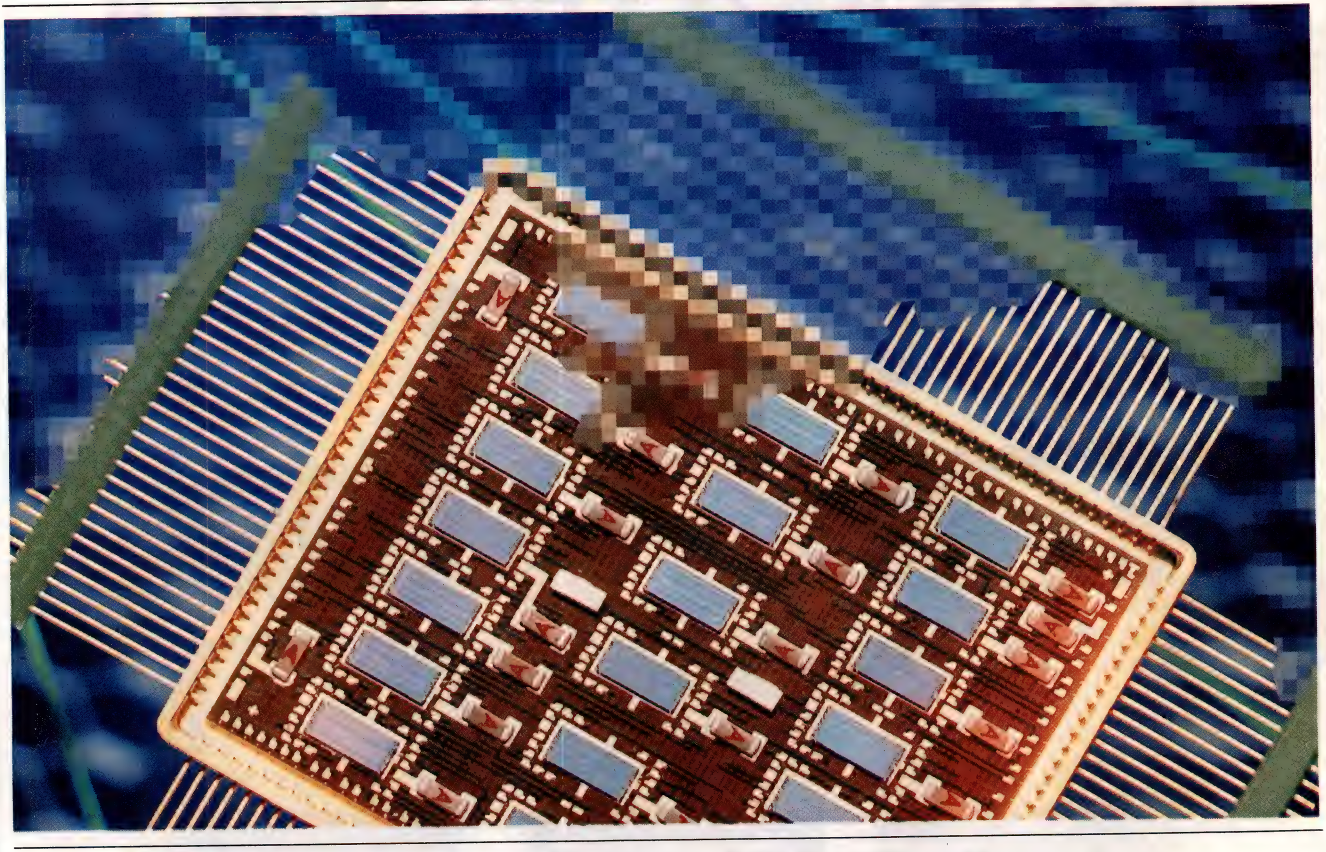

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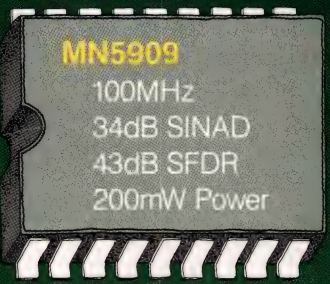

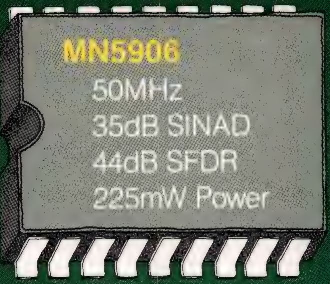

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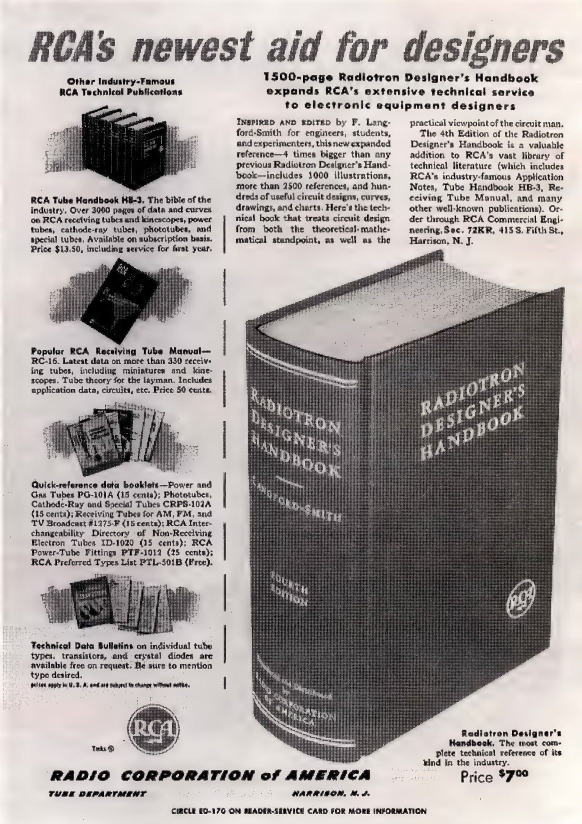

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It's not our usual policy to cover advertisements in this column, but we couldn't pass up the opportunity to recall this landmark book: 1500 pages of densely packed practical engineering design information. We suspect, however, that it didn't have the lifetime it deserved because of the industry's subsequent shift to transistors.—Ed.

Analog Computing Unit Incorporates 10 amplifiers

The Model HK Operational Manifold Component comprises a set of 10 Model K2-W Operational Amplifiers plugged into a special chassis to form a basic Analog Computing facility. All common service connections are provided. An arrangement of computing connections is featured in which circuit elements and input and output leads are readily plugged in to form feed back circuitry. Positive and negative inputs to each amplifier, both at high impedance, are available. Of the four amplifier poles comprising plus input, minus input, output, and ground, the jacks for every pair are spaced on 3/4" centers for double banana plugs. Speeds of computation range from a repetitive or single-shot period of 0.001sec down to a solution time of many minutes. Power required is ±300v d-c at 50ma, and 115v a-c at 0.5 amp. George A. Philbrick Researches, Inc., 230 Congress St., Boston 10, Mass. *(Electronic Design, November 1953, p. 24.)*

The decades of the '50s and '60s were the heyday of analog computers, which offered a simple but elegant solution to a linear differential equation, and Philbrick was at the forefront. Regular readers may recall that our June 27, 1991 cover showed the Philbrick K2 amplifier as a background to Apex Technology's then new high-voltage op amp. —Ed.

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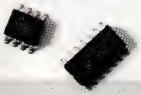

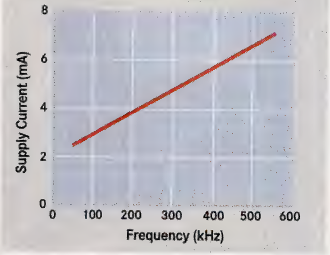

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	KM6164002	256K×16	20/25	SOJ(R)	'93,3Q	
	KM64V4002	1M ×4	20/25	SOJ(R)	'93,2Q	3.3V
	KM68V4002	512K×8	20/25	SOJ(R)	'93,2Q	3.3V
	KM616V4002	256K×16	25	SOJ(R)	'93,3Q	3.3V
1M	KM64B1003	256K×4	10/12	SOJ(R)	NOW	BiCMOS
	KM68B1002	128K×8	10/12	SOJ(R)	NOW	BiCMOS
	KM641003	256K×4	15	SOJ(R)	NOW	
	KM681002	128K×8	15	SOJ(R)	NOW	
	KM6161002	64K×16	15	SOJ(R)	NOW	
	KM64V1003	256K×4	15	SOJ(R)	'93,3Q	3.3V
	KM68V1002	128K×8	15	SOJ(R)	'93,3Q	3.3V
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	KM658512	512K×8	80/100	SOP/TSOP	NOW	Pseudo
1M	KM681000	128K×8	70/85/100	DIP/SOP/TSOP	NOW	
	KM658128	128K×8	80/100	DIP/SOP	NOW	Pseudo

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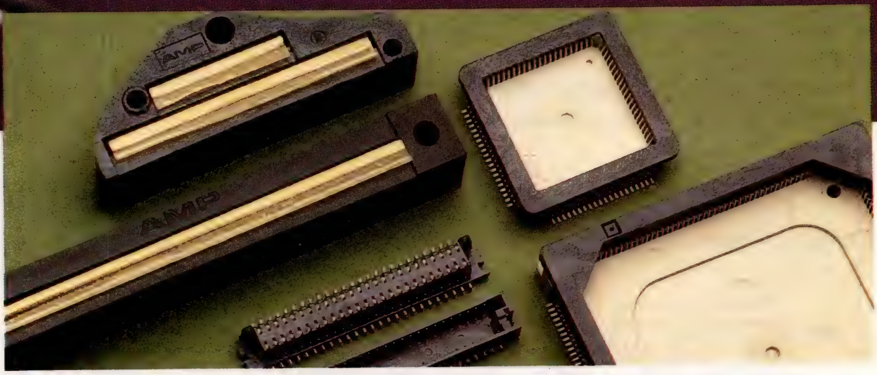

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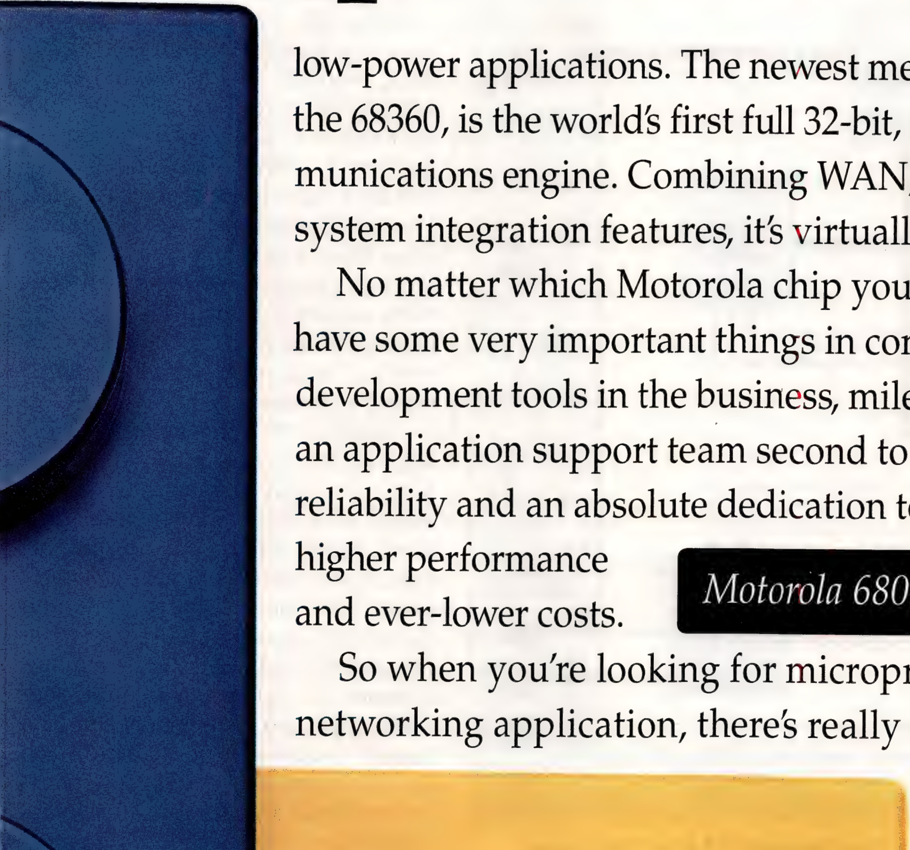

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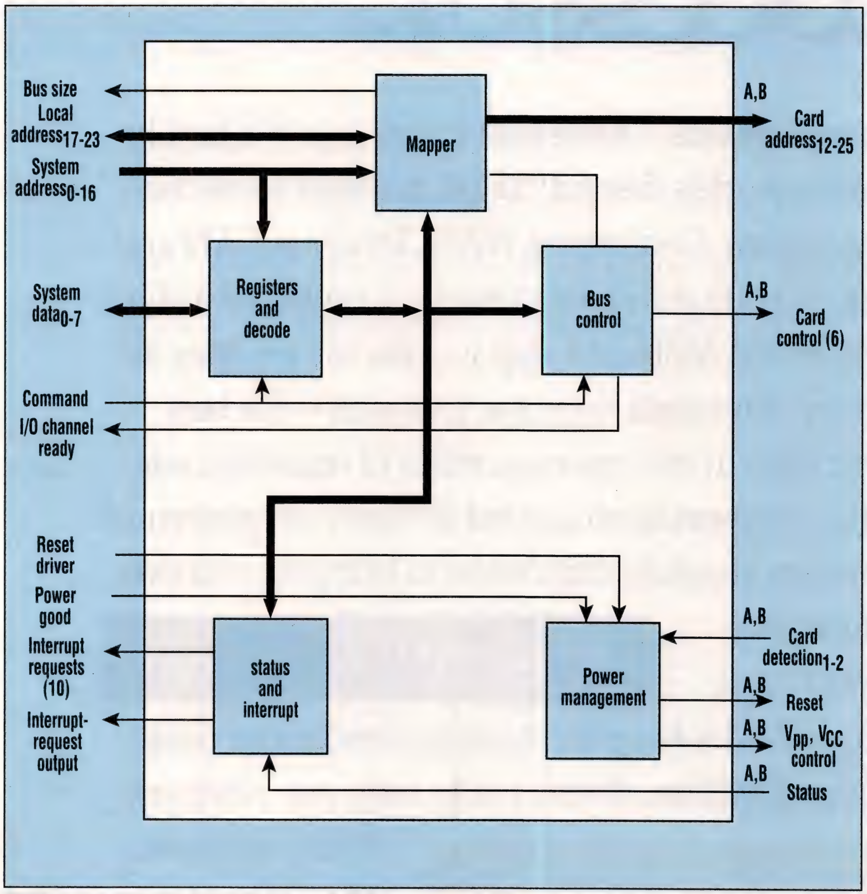

2. PORTABLE COMPUTERS can take advantage of 3.3- or 5-V devices using Vadem's VG-365 PCMCIA controller. The chip, which supports up to eight slots with no external logic, maintains compatibility with PCMCIA Release 2.01, JEIDA 4.1, and the ExCA extensions.

Wave-table synthesis is very straightforward and fairly easy to design with, hence its popularity. Waveguide synthesis, on the other hand, suffers because of the processing power that's required to handle the complex equations. For example, to compute each sound, the equation must be calculated to process every point in the waveform. But, with processors increasing in computational power, it's becoming less of an issue.

In taking a closer look at waveguide synthesis, it has the ability to set up a physical model of a sound and then alter it. The technique, called sound rendering, offers a fundamentally new way of looking at sounds. It's possible to create a program that could in turn create and play new and unthought of instruments, such as a guitar with a 4-ft. neck. This isn't something anyone would likely build, but with waveguide synthesis, users can create that sound. Some instrument companies, such as Yamaha, are investigating whether it's feasible to use waveguide synthesis in keyboards. Though that type of product wouldn't be as cost-effective as a mainstream consumer-level PC product, price issues aren't as sensitive in that market.

Media Vision Inc., Fremont, Calif., a leader in waveguide development, feels that it can implement the technique and keep it at the consumer-pricing level. The company is presently designing a custom ASIC that can perform the needed processing power (the target date for the chip is early next year). In addition to the custom DSP chip, the waveguide-based board requires a digital-to-analog converter to produce the analog sound, as well as some RAM. Media Vision's board will also be able to perform wave-table synthesis, because they're more suitable for particular sounds, such as those created by percussion instruments.

Although waveguide synthesis seems to be the technique of the future, several recent advances in wave-table synthesis indicate that it's likely to be around for some time. Previously, simple wave-tables had one loop point to represent a sound. That point was repeated to sustain a note. Newer technologies employ a multi-segment wave table that contains separate attack, loop, and release portions of the waveform. As a result, the accuracy of the overall sound is increased, because different portions of a note contain different sounds. For example, in a piano note, the first 100 ms carries the sound of a felt hammer striking a steel string. That's the attack portion. Then, there's a repeated sound, called the loop. Finally, the note fades out, causing the release. Enhancements in DSP chips are making it easier to implement the multi-segment approach. Such chips can also handle cycle-acoustic effects, such as reverb and delay, which previously were only found on professional-quality sound boards.

Media Vision will be displaying its current audio product, called Memphis, at Comdex. Memphis is a self-contained multimedia upgrade component system that fits under or beside a PC's monitor. Two models are available, representing two different speaker types. The system integrates all of the external wiring into one cable. The other components include a ProAudio Spectrum sound board and a double-speed NEC CD-ROM drive.

Designs based on the EMU8000 architecture offer high-quality audio in a cost-effective, easy-to-install package. The EMU8000, from E-mu Systems, Scotts Valley, Calif., consists of three elements—an integrated audio digital-signal processor, a sound-file library, and control software. Boards built with this architecture can include a MIDI interface, user-definable digitally-sampled sound libraries, built-in digital effects and audio filtering, and 32-voice polyphony. Such applications that suit the EMU8000 architecture include kar-

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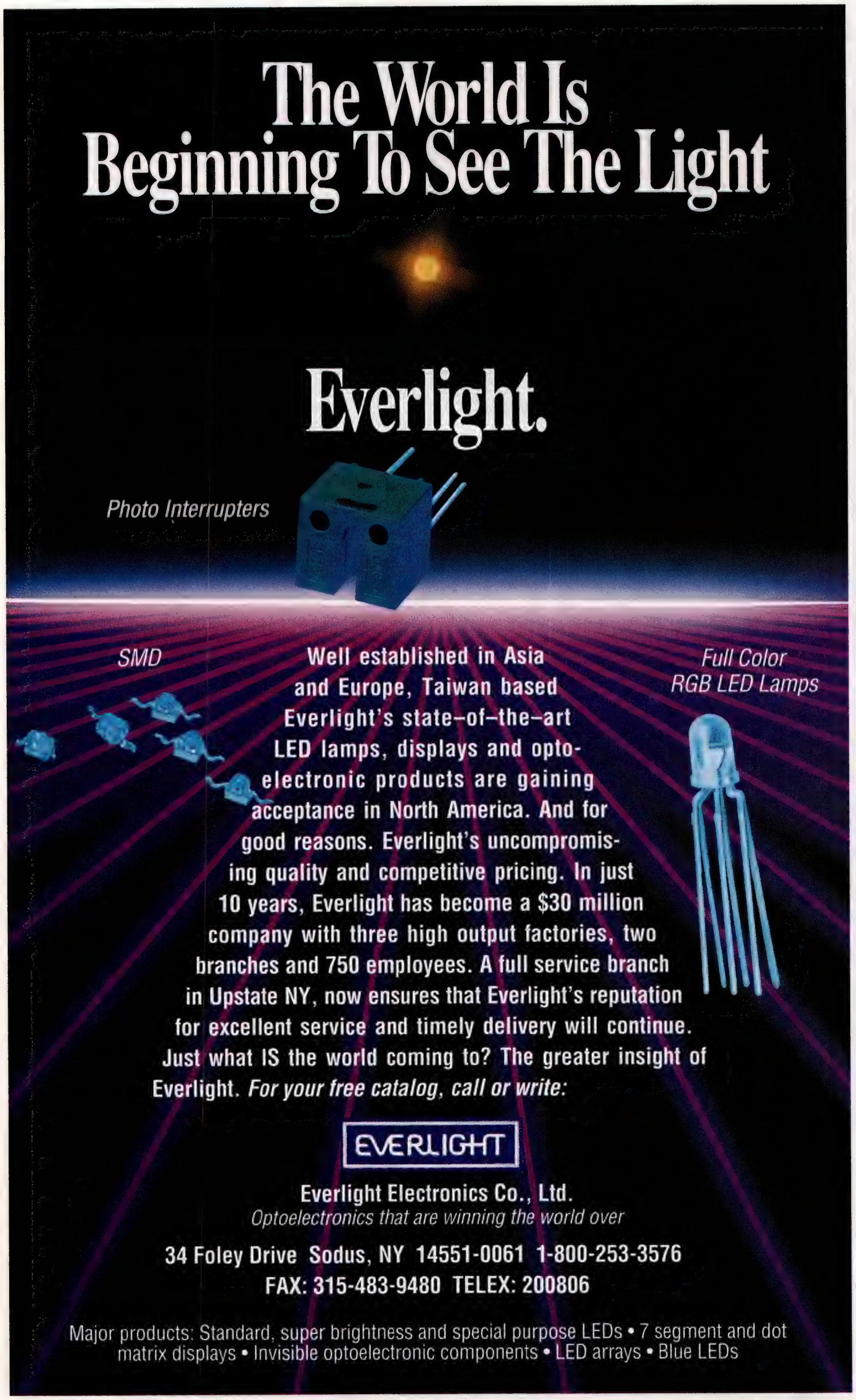

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PCMCIA LETS IT GO

PCMCIA systems, drives, and peripherals are sure to garner a fair share of attention at Comdex. Designers of PCMCIA-based systems can implement either 3.3- or 5-V parts using the VG-365 controller designed by Vadem Inc., San Jose, Calif. The part is compatible with the PCMCIA Release 2.01 and JEIDA 4.1 specifications, and complies with the ExCA extensions for interchangeability. Two sockets are supported, but the device can be cascaded to handle up to eight sockets without any external logic. Using external decoder logic, unlimited cascading is possible. The part can handle I/O and memory cards, including rotating and solid-state hard-disk drives.

The VG-365's bus controller supports the system-bus timing of standard ISA and EISA architectures, including those based on an Intel 386SL microprocessor *(Fig. 2)*. A programmable configuration mechanism lets designers control the card setup either in software or firmware. The chip is housed in a 160-lead quad flat pack.

Portable-system users are never out of touch using the AccessCard, a PCMCIA-based one-way message receiver from Wireless Access Inc., San Jose, Calif. The card, with its built-in antenna, acts like a pager and works with popular messaging services, including all 900-MHz carriers. The card, which fits a Type 2 form factor, is initially compatible with Hewlett-Packard's HP100LX and Casio's Z-7000 handheld computers. The AccessCard is based on a DSP architecture that turns parts of the card on and off to help extend the life of the PCMCIA card's internal battery.☐

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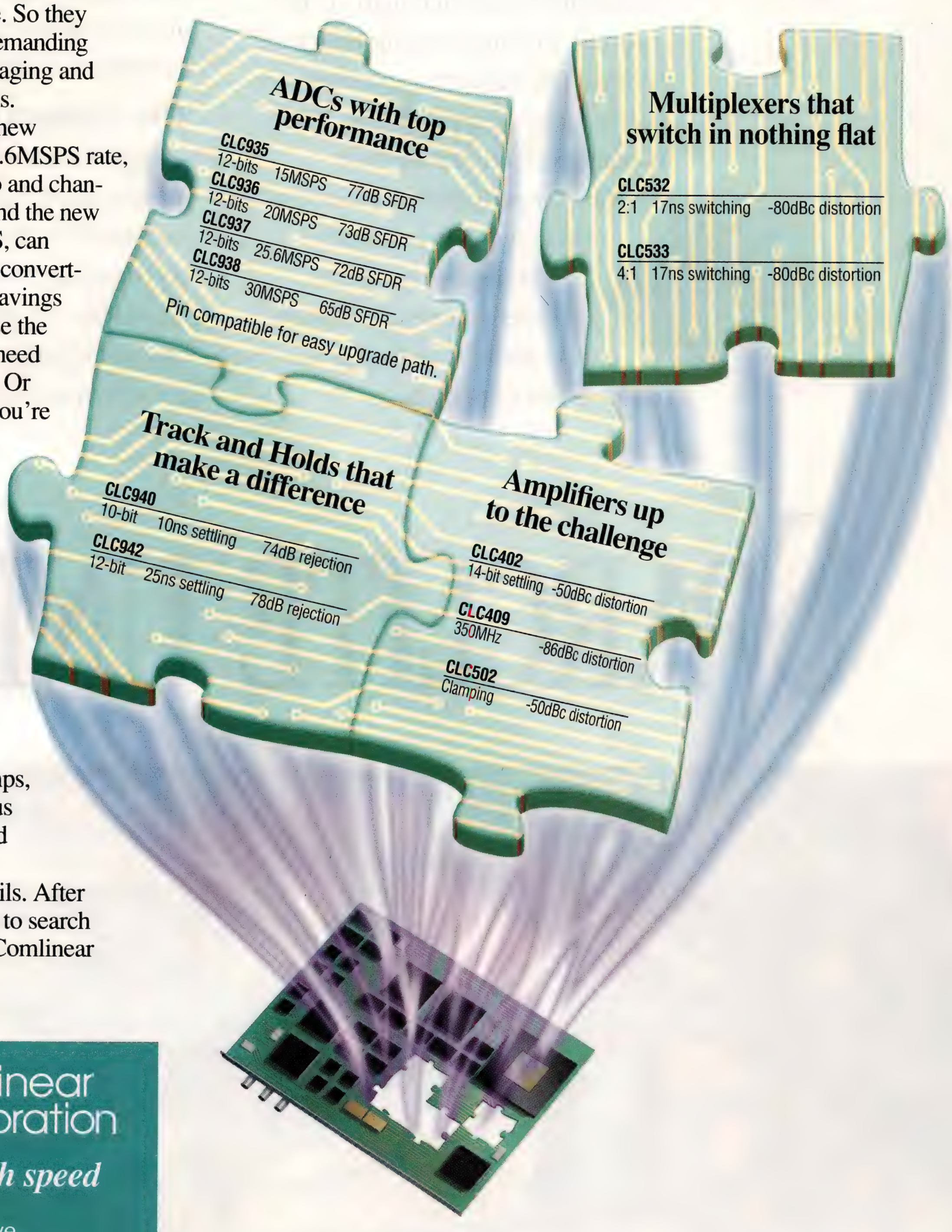

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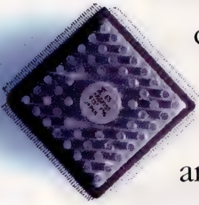

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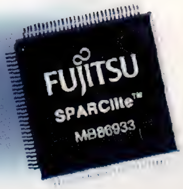

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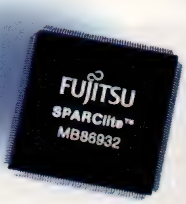

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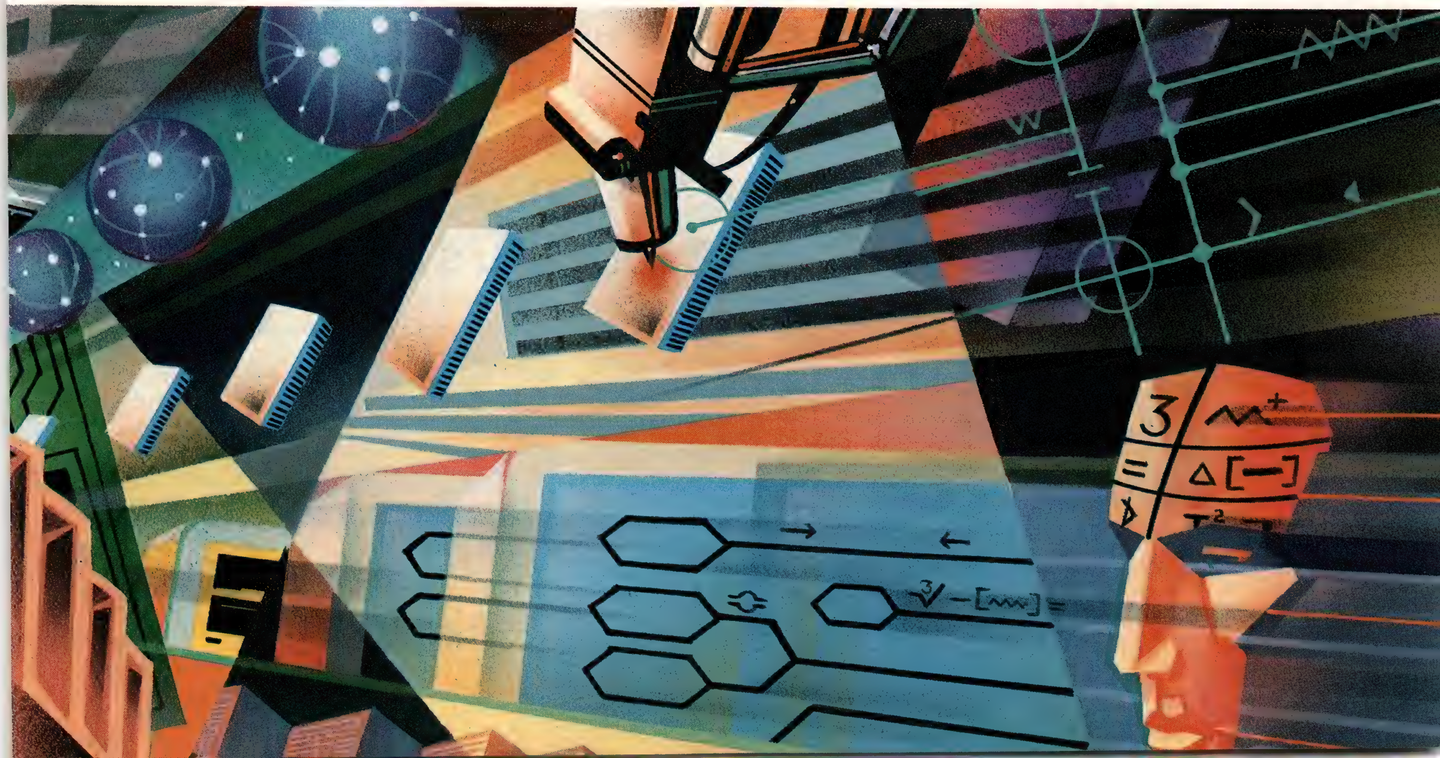

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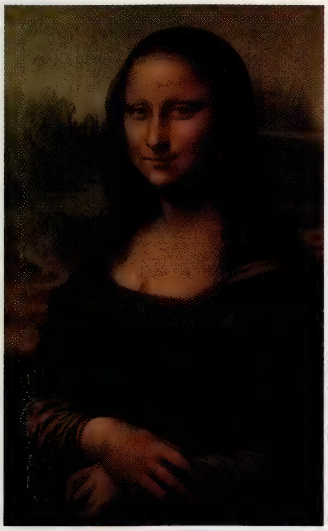

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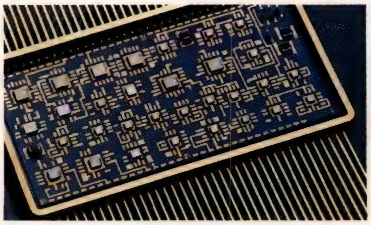

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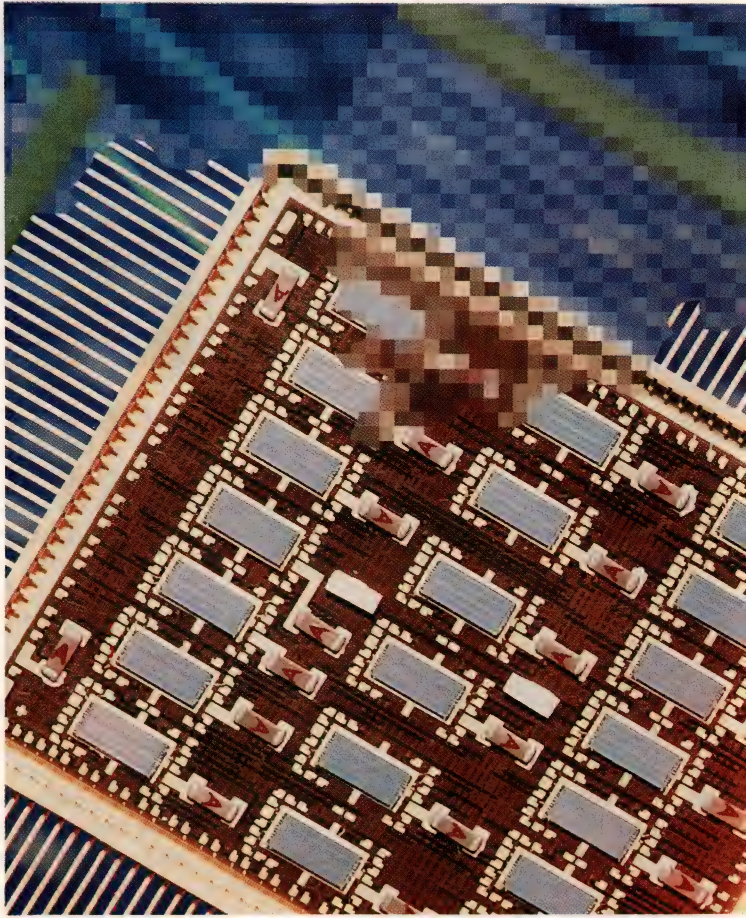


Although many system designers see multichip modules (MCMs) as the ticket to pushing today's ultra-fast ICs to their theoretical performance limits, most shy away from the technology for a number of reasons. Chief among those is the fact that unlike other technologies initially developed for high-end computers and military systems, the MCM remains prohibitively expensive for designers of commercial systems.

In addition, each of the existing MCM-substrate technologies—deposited thin-film substrates (MCM-D), ceramics (MCM-C), and laminates (MCM-L)—comes with cost and performance trade-offs that make choosing a substrate a frustrating process. If a given substrate isn't too costly for a particular application, then its performance isn't up to the silicon's signal-propagation demands. If the cost is in line with the budget, then the substrate can't support the routing density the circuit requires.

In trying to find a middle ground, Packard-Hughes Interconnect, Irvine, Calif., came up with a laminated-film (MCM-LF) substrate technology. This alternative method approaches the speed and density potential of the high-end options, MCM-C and MCM-D, while keeping costs closer to the MCM-L end of the scale *(Fig. 1)*.

The laminated-film technique offers numerous advantages that can streamline the process of MCM implementation while finally making it a viable option for commercial users. Against the high-performance MCM-D and MCM-C technologies, the MCM-LF technology compares most favorably in terms of cost and manufacturability. Against the lower-cost MCM-L technology, it shines in terms of performance.

MCM-D substrates are fabricated on IC-manufacturing equipment by depositing alternating layers of metal and polyimide dielectric. These are applied to a silicon-wafer base, which brings with it all of the attendant yield problems associated with IC manufacturing. When spinning on the liquid polyimides, which can cost as much as $400/gram, a large percentage of the material is wasted in the process. The whole procedure must be carried out in clean rooms, which further drives up the cost. Moreover, the sequential, additive nature of the process means that the substrate can't be fully tested from an electrical standpoint until it's completed.

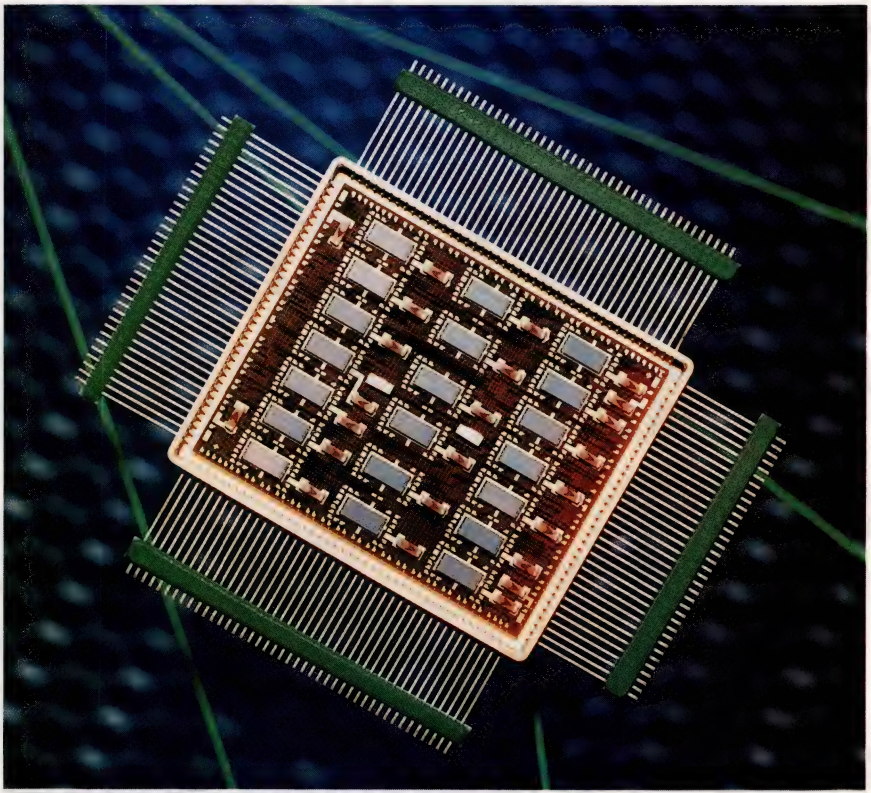
Ceramic substrates are also additive and sequentially processed, so the same testing difficulties apply. The materials, such as green tape, are expensive, as is the gold metallization that's typically applied to the successive layers. Substrate shrinkage during sintering sometimes causes problems as well. In addition, the capital equipment required to create ceramic substrates is costly, much like the IC equipment used in MCM-D processing.

ASSEMBLY ASSETS

The MCM-LF approach addresses these deficiencies from various fronts. MCM-LF substrates consist of layers of a modified polyimide film. The layers are processed individually and then laminated together in a final step. This offers the advantage of being able to electrically test each layer before committing them to final assembly. Furthermore, the materials and capital equipment required for MCM-LF fabrication are typically far less costly than for either MCM-D or MCM-C technologies.

The modified polyimide film has a dielectric constant of 3.4 and can be laminated at half the temperature required by earlier polyimides. This results in a substrate with less stress. In addition, the film is only about 18 μm thick, which allows heat to be dissipated through the base substrate without using thermal wells (except in the most extreme cases of the largest ICs).

One measure of an MCM substrate's worth is the efficiency of signal routing in the Z axis. In a typical pc board, through-hole vias take up huge areas and waste valuable routing area on inner layers. With MCMs, short optimized signal paths are a must. The density of staggered blind and buried vias that each technology makes possible helps to achieve such paths. The diameter of the vias and the relative ease or difficulty associated with their creation is the main determinant in the module's density and, ultimately, its cost.



1. LAMINATED-FILM (MCM-LF) substrate technology approaches the speed and density potential of the high-end options, MCM-C and MCM-D, while keeping costs closer to the MCM-L end of the scale.

For those seeking to implement an MCM while keeping costs down, the clearest option is MCM-L technology. However, the overriding deficiency of MCM-L substrates is their via sizes. According to Christopher Schreiber, senior development engineer at Packard-Hughes, conventionally drilled vias run about 12 mils in diameter in MCM-L. Although smaller vias are possible, they become expensive to produce at about the 8-mil-diameter range.

In contrast, the modified polyimide films used in MCM-LF substrates permit laser drilling of vias of less than 5 mils *(Fig. 2)*. In MCM-LF technology, vias can be created with the company's Gold Dot electrodeposited raised bumps. Where raised bumps are used, a metal-laden epoxide provides the signal path between layers.

If they wish to throw cost to the wind, MCM-L users can achieve via diameters of 3 mils by turning to lasers or computerized numerical-control (CNC) micropunches. But that won't fix the other performance drawbacks inherent to MCM-L technology. The coefficient of thermal expansion (CTE) mismatch between the silicon die and substrate, the glass-transition temperature (T_g) of materials, and bondability of the gold metallization, are all major areas of concern.

COST COMPARISON

The various cost and performance trade-offs among MCM-LF and MCM-L, MCM-C, and MCM-D are best illustrated by a test case. According to Schreiber, in cost terms, MCM-L leads the pack at about \$1 per square inch per conductive layer. MCM-LF and MCM-C follow at about \$3/in.^{2}/conductive layer, and MCM-D trails at about \$15/in.^{2}/conductive layer. The true measure of cost, however, is in routing efficiency, in which via sizes and line widths play the largest roles.

Working from the test case of a relatively complex DSP circuit, Packard-Hughes's engineers first attempted routing the circuit in

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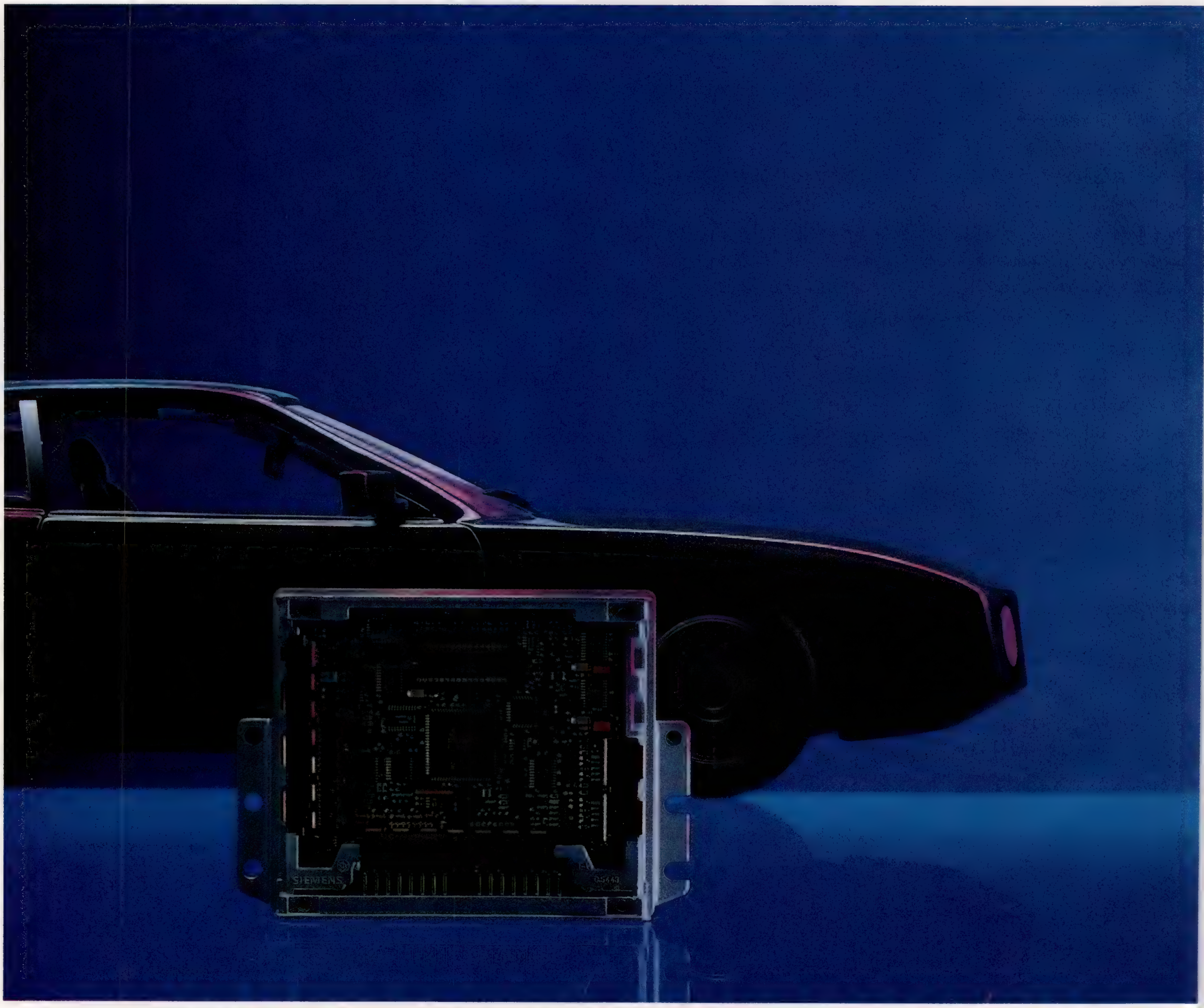

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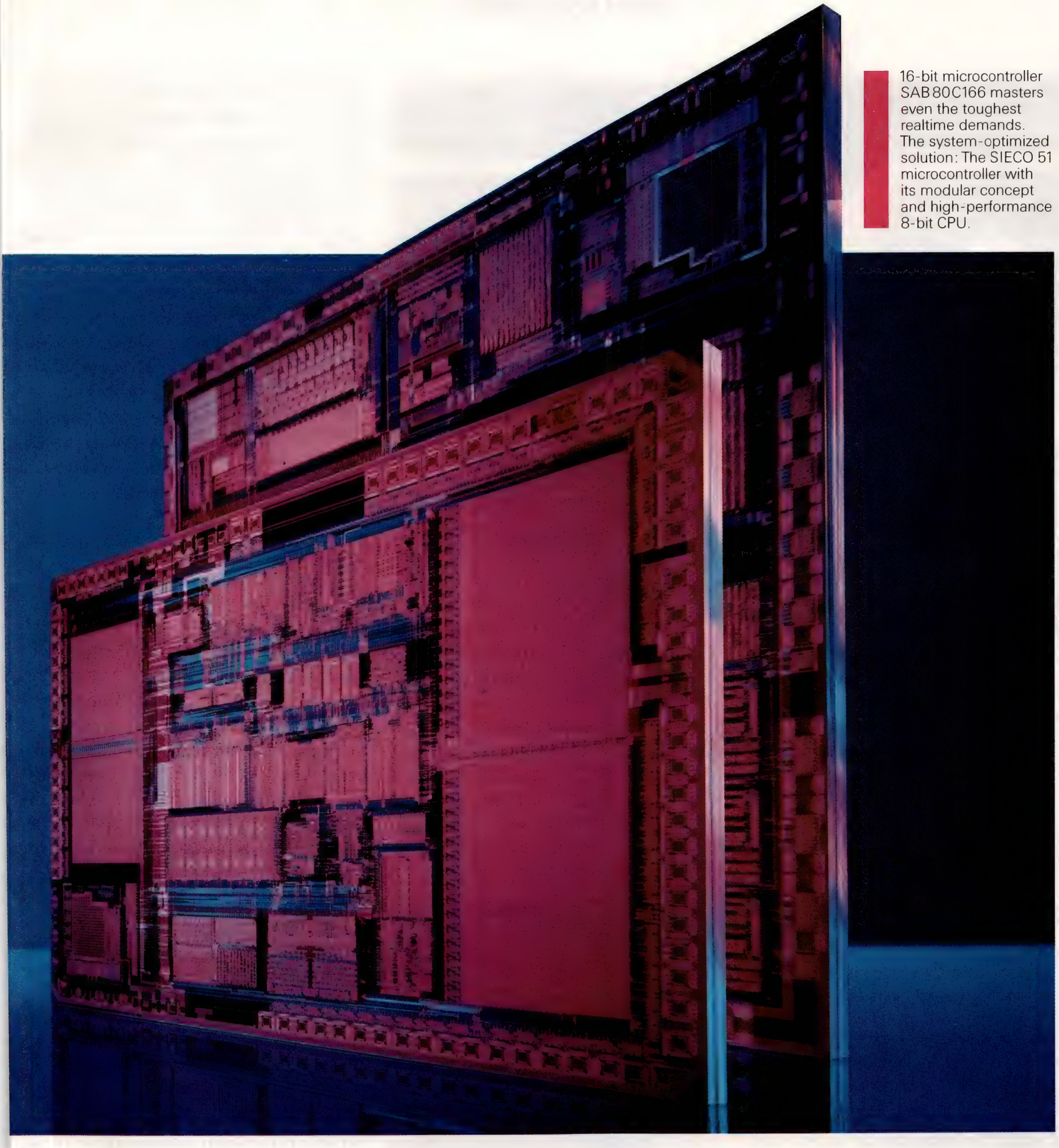

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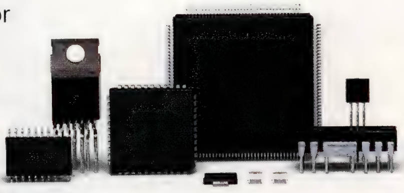

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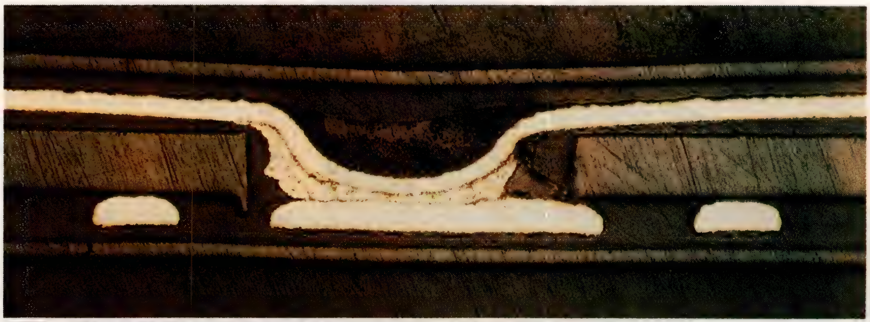


2. VERY SMALL-DIAMETER VIAS are possible with the MCM-LF technology. This 200X micrograph shows an electrodeposited inner-layer via with a diameter of 0.0015 in. The via was defined using an excimer laser.

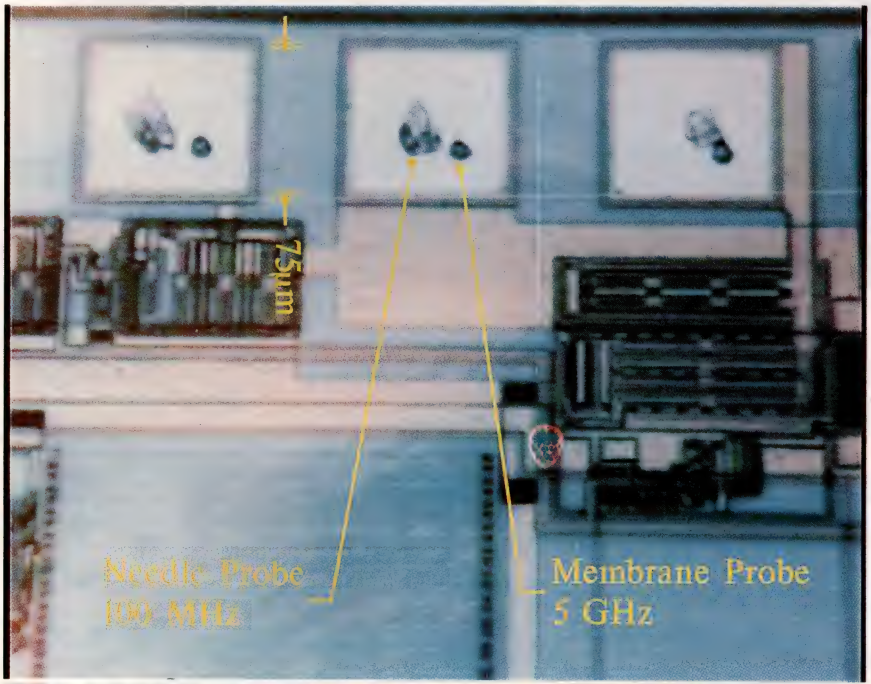
MCM-D technology, which was accomplished in five layers. Extrapolating from the cost figure of $15/layer, that means that a 1-in.^{2} module would cost roughly $70. In MCM-LF technology, the same module was routed in nine layers for a cost of about $30. In MCM-L technology, the module was routed in 17 layers.

According to Schreiber, although the MCM-L version would cost less than $20, it's extremely unlikely that an MCM-L module with so many layers could be made to function on the first attempt, if at all. For its part, implementing the same module in MCM-C, which also requires 17 layers, would be likely to produce a functional substrate but at a relatively high cost of about $50.

The end result for MCM-LF, in this test case, is a routing density that falls between that of the two high-end technologies but at a cost that's lower than both. On the other hand, the low-cost MCM-L technology probably wouldn't be up to the task, so its cost becomes a non-issue.

Besides its cost-performance balance, MCM-LF technology offers other significant packaging advantages when compared with the alternatives. In high-end electronics packages using die stacks, Packard-Hughes demonstrated the ability to share one decoupling capacitor placed directly behind the stack. Being able to place decoupling capacitors on the opposite side of the MCM delivers several distinct advantages that other technologies cannot. The most important is that it reduces line length, inductance, and ground bounce. It also provides a balanced construction that places the capacitor equidistant between power and ground. Even if one were able to place decoupling capacitors adjacent to the die on a single-sided MCM, there would be no assurance of their optimal placement relative to the power and ground lines.

Yet another advantage is gained by virtue of the technology's additive processing. By forming the circuit traces on each layer in this manner, superior control over conductor geometries is possible. This, in turn, enhances control of lead reactance, crosstalk, and pulse-shape characteristics. While subtractive methods of circuit formation (etching) yield conductors with a trapezoidal cross section, the additive method provides truly rectangular conductors. The ability to exactly control the conductor geometry facilitates controlled-impedance transmission lines, which minimizes signal reflections and ringing.



3. A MEMBRANE PROBE for verifying known-good die under development at Packard-Hughes will provide at-speed testing with 80-ps edge speeds and a lifespan of over 350,000 touchdowns. The probe's soft contact with die pads generates less particulates and, therefore, requires less frequent cleaning.

INFRASTRUCTURE ISSUES

In addition to the MCM-LF technology itself, Packard-Hughes is engaged in other development projects that address the wider infrastructure concerns held by many would-be MCM implementers. Anyone who's tried to design and build an MCM knows that producing a functional substrate is only half the task. Acquiring bare die, testing them, and populating the substrate is beyond the scope of all but the most vertically integrated companies.

Because successful MCM production depends on having good die, several methods are currently used to make bare die testable. Among the most common is inner-lead bonding (ILB) to a tape-automated-bonding (TAB) leadframe. Unfortunately, ILB calls for the plating of bumps on the undiced wafers. The availability of bumped die as well as the risks associated with bumping functional wafers often outweighs the advan-

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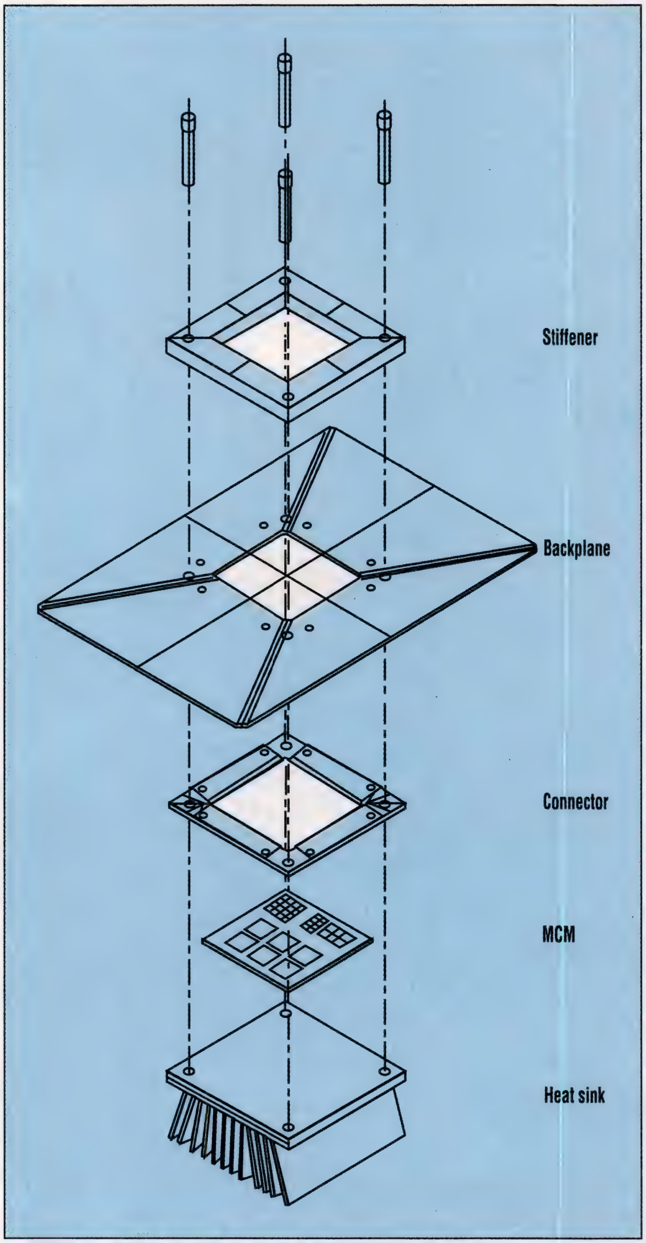
tages of this method.

Hughes Research Laboratories, Malibu, Calif., came up with a method for verifying die integrity, which is being shaped into a commercial product at Packard-Hughes. The Packard-Hughes membrane probe is currently qualified at several major IC manufacturers' facilities. Besides providing "at speed" testing of ICs on a 0.004-in. pitch, this technology doesn't plow into the pad as do tungsten needle probes. The result is a minimum of particulate generation and subsequent cleaning *(Fig. 3)*.



4. THE GOLD DOT TECHNOLOGY created by Packard-Hughes can provide an interface capable of the densities required by MCMs without the signal degradation inherent in other interconnection methods. The Gold Dot-based connectors represent a convenient means of removing and replacing modules in the field.

The ability to perform at-speed testing is made possible by a bumped membrane constructed in a microstrip configuration. Recent tests have demonstrated an 80-ps device edge speed. Moreover, alignment of the bumps to the IC pads remains consistent throughout the probe's 350,000-touchdown life, which eliminates the need to tweak, clean, and align sensitive and delicate needles.

A second development area addressed by Packard-Hughes is that of the interconnection between the MCM and the motherboard. As MCMs gain functionality, more I/Os are required, and Packard-Hughes' Schreiber believes that all MCMs now being designed exceed today's standard pin-and-socket interconnection densities of 20 pins/linear inch (0.050-in. pitch). In addition to the density problem, the operating frequencies of those MCMs is generally 50 MHz and higher. At such frequencies, a poorly designed interconnect between the MCM and its motherboard can seriously degrade performance and introduce noise.

The company's Gold Dot technology offers an interface capable of the required densities without the signal degradation inherent in other interconnection methods. Also, the Gold-Dot-based connectors represent a convenient means of removing and replacing modules in the field. This function simplifies maintenance and repair of systems using MCMs, and facilitates potential design upgrades.

A typical MCM assembly consists of the stiffener, multilayer backplane, Gold Dot connector, populated MCM, and heat sink *(Fig. 4)*. Here, too, significant cost savings can be realized with respect to conventional approaches. For example, a ceramic package that can provide a hermetic interconnect for a 2-by-4-in. substrate costs $750 (about $0.70 per I/O). The Gold Dot approach offers a dematable solution for about $0.30 per I/O.

Although the ceramic package provides hermeticity, the populated substrate must be glued into the package and all I/Os must be wirebonded between the substrate and the package. Then, the package must be electrically tested before its lid is welded on. After testing and lid attachment, the package is soldered to its backplane.

If a die in such a hermetic package fails in the field, the backplane must be removed, the package unsoldered, and the substrate removed from within. This is an extremely delicate procedure. In most cases, the package itself is sacrificed by being sawed apart so that a blade can be used to gently pry the substrate from the package. In Schreiber's opinion, the advantages in terms of ease of assembly offered by the Gold Dot approach outweigh even the cost advantages that it offers compared with the ceramic-package approach.☐

PRICE AND AVAILABILITY

Pricing for multichip modules implemented in MCM-LF technology is expected to be in the range of $3/in.^{2}/conductive layer in volume. Nonrecurring-engineering charges are estimated to be from 25% to 33% of those imposed by competing MCM technologies. The process will be ready for production by the beginning of 1994.

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CIRCLE 203 FOR U.S. RESPONSE

CIRCLE 204 FOR RESPONSE OUTSIDE THE U.S.

"If you doubt the power of advertising I suggest you consult a doctor."

Don't find out colon cancer is curable too late in life.

Herb Baum, Pres., Campbell North & South America and Chm. of the Advertising Council.

"Colon cancer is a disease that afflicts more than 150,000 Americans each year and eventually kills over half. Yet, any doctor will tell you that with early detection, the survival rate could be raised to as much as 90%.

Can advertising have the power to make people confront this disease, overcome their fear and actually consult their doctors about it?

You bet your life it can.

Take the case of the Advertising Council's campaign against colon cancer. The first-ever study of public service advertising that actually isolated the impact of advertising from other market elements like the news, editorials and public relations.

Research was conducted from July 1989 to July 1990 in 4 markets in 10,000 households, at the equivalent of $21.3 million worth of air time, the average amount of donated time behind Advertising Council spots.

After six months of being exposed to one commercial, awareness of colon cancer among adults 40 and over rose from 11% to 29%.

After a year, awareness reached 40%.

The number of men who consulted their doctors more than doubled to 15%.

Now, if advertising can get people to see their doctors about something as unpalatable as colon cancer, don't you think it can get people to consider your product?

Oh, there's one more thing. If you're over 40, ask your doctor about colon cancer."

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This advertisement was prepared by Calet, Hirsch & Ferrell, Inc., New York, New York: Photo: Fred Weber.

"The remarkable thing is, when you think about McDonald's® you've got to think about people. A friendly crew person welcoming you. Kids, moms and dads having a good time at McDonald's, even a funny clown named Ronald.® Those pictures in your mind are advertising at work.

"Without advertising, everybody would think Ronald was just the name of a former president."

Mike Quinlan, Chairman, CEO McDonald's (left)

Our advertising is people to people—an invitation from our people to our customers to come in and visit. Personal, friendly, and above all, real.

I'm told there are business people out there who don't believe in the power of advertising. For them, two facts: First, McDonald's is one of the most advertised brands on this planet. Second, McDonald's is the only company listed in the current Standard and Poor's 500 to report combined increases in revenues, income, and earnings per share for more than 100 consecutive quarters since 1965.

Frankly, Ronald and I like to think there's a connection here."

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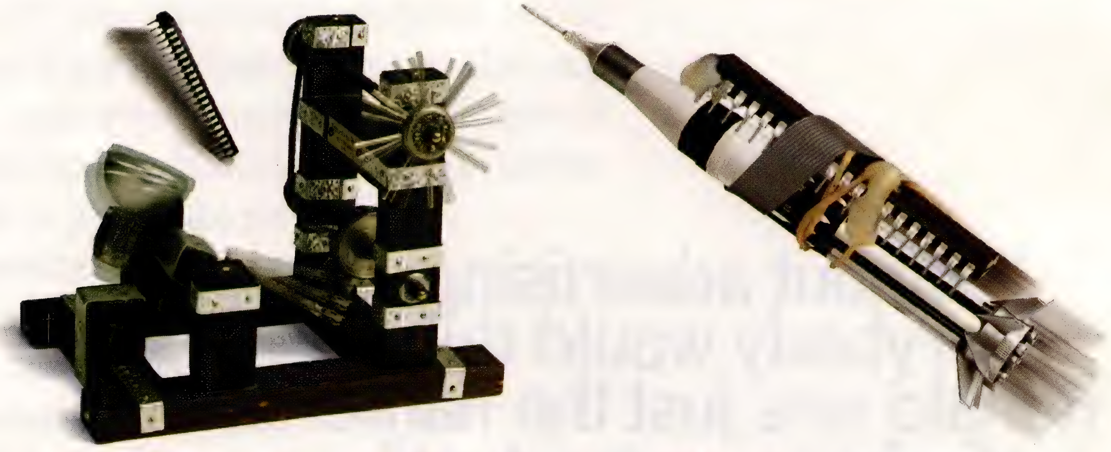
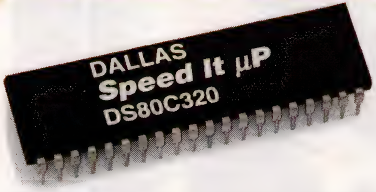
Running out of tricks to make the 8051 go faster?



Try the only 8051 built for speed.



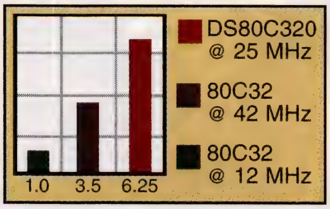
Since its introduction a short time after the dark ages, the 8051 hasn't really improved. Until now. The DS80C320 High-Speed Micro runs up to three times faster than other 8051s using the same crystal.

Fewer Clocks for Greater Performance

We redesigned and updated the architecture using four clocks per instruction instead of the usual 12. You needn't be a math whiz to figure out that when the same instruction takes 1/3 the clocks, software can do more in less time.

Drop In For Speed

The DS80C320 is a drop-in replacement for 80C31- or 80C32-based designs. So you can plug it into your system with no redesign and get an instant performance improvement, regardless of the speed at which your system runs. With an adjustable speed interface to RAM and peripherals, the DS80C320 is easy to adapt to existing hardware.



The DS80C320 outperforms other 8051s even when they use higher clock speeds. A DS80C320 running up to 25 MHz can do almost twice as much work as a standard 8051 running at over 42 MHz.

At its top speed of 25MHz, the DS80C320 performs an instruction cycle in 160 ns. And you can look for higher speeds from Dallas soon.

Long-Awaited Improvements

But speed isn't the only improvement we've made. For example, we've added a Dual Data Pointer. A second, full-function UART that is completely independent from the original. Six external interrupts instead of the usual two. A power monitor that provides early-warning interrupt and power-fail reset. Even a programmable watchdog timer.

The DS80C320 offers all these features, with no external components, in the standard pinout. It's still fully 8051 instruction set-compatible and offers the familiar 256 bytes of RAM and three 16-bit timers.

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CIRCLE 112 FOR U.S. RESPONSE   CIRCLE 113 FOR RESPONSE OUTSIDE THE U.S.

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IMPROVED DSP ICs EYE NEW HORIZONS

DAVE BURSKY

ENHANCED DSP CHIP ARCHITECTURES MAKE MULTIMEDIA AND HDTV SUBSYSTEMS PRACTICAL BY PACKING LOTS OF PUNCH IN ONE CHIP.

Digital - signal - processing (DSP) technology has invaded nearly every aspect of design across a wide spectrum of applications. From creating multimedia graphics and audio subsystems to data-acquisition systems and consumer goods such as games and automotive controls, DSP technology has become indispensable. The extensive array of general-purpose and dedicated DSP chips now available satisfies simple as well as increasingly complex applications. And many more are on their way to help mitigate the increasingly tougher processing requirements of new applications.

Commodity DSP chips that resemble microprocessors now include 16- and 24-bit integer processors, as well as 32-bit floating-point processors that can deliver throughputs ranging from about 1 MIPS to over 50 MIPS and 120 MFLOPS. At the board level, multiple DSP chips on a card, such as arrays of TMS320C40s from Texas Instruments Inc., or even some high-throughput RISC processors (like the i860s from Intel Corp., interconnected with crossbar switches), are used in tandem as an array processor.

The arrays of multiple DSP or high-throughput RISC chips are typically used for graphics image manipulation, ray tracing, and other high-speed applications containing large blocks of data for processing. Companies are also investigating the use of neural-network and fuzzy-logic approaches to implement applications previously handled by DSP ICs *(see "DSP ICs, parallelism, and neural networks," p. 78).*

Dedicated-function chips, such as finite-impulse-response (FIR) filters, fast-Fourier-transform (FFT) processors, and JPEG and MPEG circuits for multimedia systems, aren't usually rated in MIPS, but rather in millions or billions of operations per second (MOPS or GOPS). By counting the number of multiplications, additions, and other operations, designers can get a pretty good estimate of performance because the chip's more highly dedicated architectures typically implement a hardwired function. Similarly, the latest parallel-processing DSP chips are also categorized in terms of GOPS, with some chips delivering between 2 and 8 GOPS to tackle real-time video or image processing.

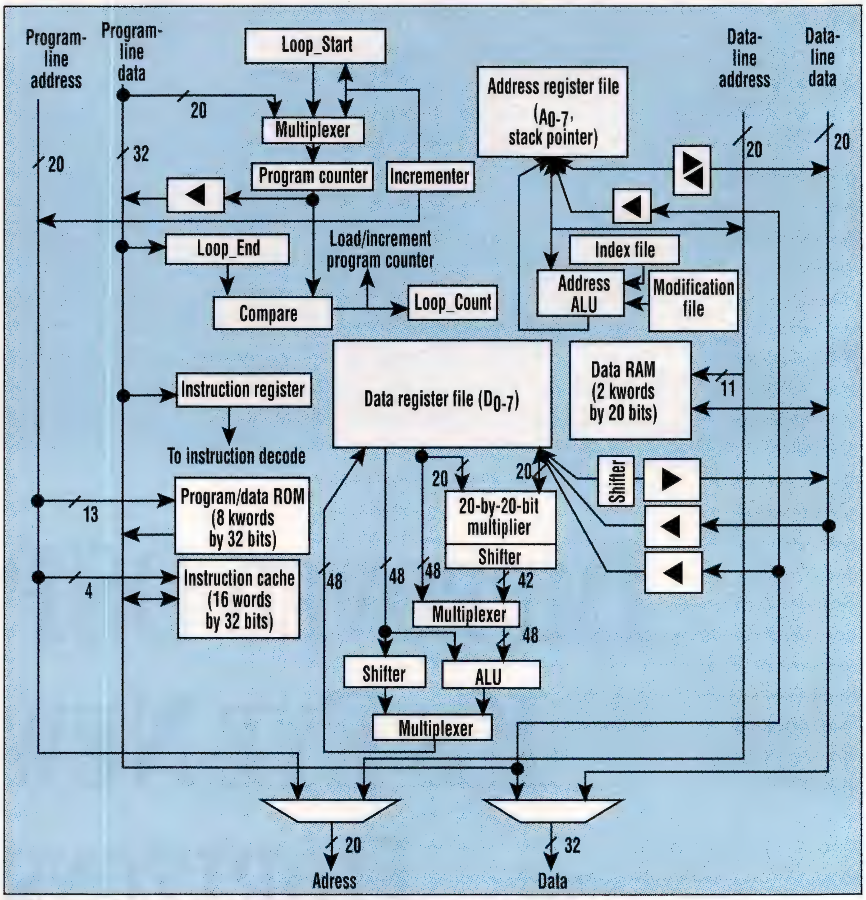
DSP functions now also serve as library cores around which designers can build application-specific processors. This is done by using support cells and resources aimed at specific market applications. Adding application-specific peripherals and memory to the core also allows engineers to create custom DSP solutions. Moreover, both the DSP silicon manufacturers and third-party software companies are adding supporting software design tools and real-time operating systems to ease the development of new applications.

Portable applications are also getting much attention these days: DSP chips are being designed into many battery-powered systems, and that means the chips must operate from low voltages and draw as little current as possible. To do that, many companies are adding power-conservation features to the chips, everything from power-down modes on CPUs to the ability to operate at low supply voltages. The operating voltage levels range from about 2.5 to 3.3 V. As a result, operating power levels of a half a watt and more have been cut to less than 30 mW during the standby mode, and even lower when the DSP IC is put inuto deep power-down modes.

MANY APPLICATIONS

Single DSP chips that can execute several million operations per second are now handling such functions as servo control. They're also handling 1200-bit/s, 2400-bit/s, and higher-speed modem communications. Microprocessor-like integer DSP chips, such as the TMS320 series pioneered by Texas Instruments, and similar chips offered by Analog Devices, AT&T Microelectronics, Motorola Semiconductor, National Semiconductor, NEC, and others, provide easy-to-program solutions. Their throughputs, though, limit their application range to system signals that have frequencies of up to several hundred kilohertz.

Forward Concepts, Tempe, Ariz., did a comparison of some key performance numbers of four floating-point processors (three DSP chips and one general-purpose RISC processor). Results showed significant computational differences among the processors, even though outwardly most of the chips are somewhat similar *(see the table)*.



1. OPTIMIZED FOR AUDIO AND MULTIMEDIA applications is the ZR38000 family of DSP chips developed by Zoran. Unlike some high-end general-purpose integer chips that use 24-bit data paths, Zoran's ICs employ 20-bit data paths for higher-quality audio than available with 16-bit versions, while keeping the cost lower than the 24-bit units. A specially designed computational block was optimized for fast-Fourier-transform processing, executing a 1024-point complex integer FFT in just 880 μs.

The performance span of today's integer DSP chips ranges roughly from about 1 MIPS to over 30 MIPS, with the higher throughput chips offering designers the ability to multitask their operations. With multitasking, one chip typically can replace several by time-sharing it among several operations. For instance, the same chip that executes fax or data-modem algorithms can also perform speech processing or other operations.

Some of the newer integer DSP ICs like the Mwave TMS320500 developed jointly by IBM and Texas Instruments and the NS32C16X family from National Semiconductor promise higher performance. Although these chips still can't handle real-time video, they can perform multiple functions that appear to be operating concurrently.

For example, the Mwave chip was recently applied to a multifunction card by Spectrum Signal Processing Inc., Burnaby, British Columbia, Canada. The AT-bus half-size card combines peripherals such as fax and data modems, a full-function digital telephone-answering machine, and 16-bit multimedia sound, all implemented by the Mwave chip running a real-time multitasking operating system.

The modem can send or receive data while sound files are playing (ELECTRONIC DESIGN, *Sept. 16, p. 131)*. National Semiconductor's

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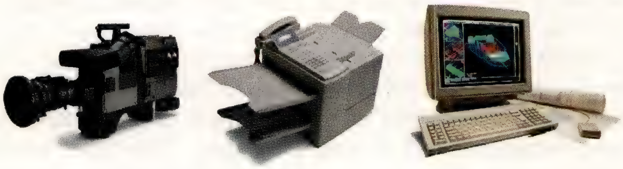

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CIRCLE 88 FOR U.S. RESPONSE   CIRCLE 89 FOR RESPONSE OUTSIDE THE U.S.

TyIn2000 card doesn't have the multitasking capability, but offers a similar array of capabilities by simply reprogramming the DSP chip for each application.

To tackle large vertical markets such as studio-quality digital audio, DSP ICs can be custom-crafted with the optimal set of on-chip resources. The just-released ZR38000 family created by Zoran Corp., for example, was designed to tackle multichannel Dolby audio for AC-3 quality compression and decompression as well as speech processing, MPEG-1, and music synthesis. To handle those applications yet keep chip area to a minimum, the ZR38000's architecture was optimized to perform 4-cycle radix-2 FFT butterfly operations and execute 25 million instructions/s *(Fig. 1)*.

A full bidirectional barrel shifter, zero-overhead nested looping, single-cycle ALU/multiplier/shifter operations, and a unified 1-Mword data/program address space allow the processor to decode six-channel digital surround sound. On-chip resources include 8 kwords of 32-bit-wide program/coefficient memory, and 2 kwords of 20-bit-wide static-RAM data storage.

The ZR38001, a variant of the ZR38000, will be offered with program RAM instead of ROM. Other variants include application-specific versions with predefined ROM code for six-channel Dolby Audio AC-3 decoding (the ZR38500), two-channel AC-3 decoding (the ZR38501), and two-channel MPEG audio decoding (the ZR38511).

With 32-bit-wide instructions, 20-bit-wide data, and a 20-by-20-bit multiplier, the ZR38000 can execute FFTs faster than any other device, save for dedicated FFT and high-end floating-point processor chips. For instance, a 1024-point complex FFT requires just 0.88 ms—about one third the time required by chips such as the Motorola DSP56002 and the TI TMS320C51. Thus, a single ZR38000 does the processing work previously done by five DSP chips operating in parallel.

The 20-bit data path gives the chip a level of precision that's located right in the middle between typical 16-bit and high-end 24-bit integer chips. At $42 each (in 1000-unit quantities), the chip produces higher quality audio than 16-bit solutions but does so at a lower cost than 24-bit DSP ICs.

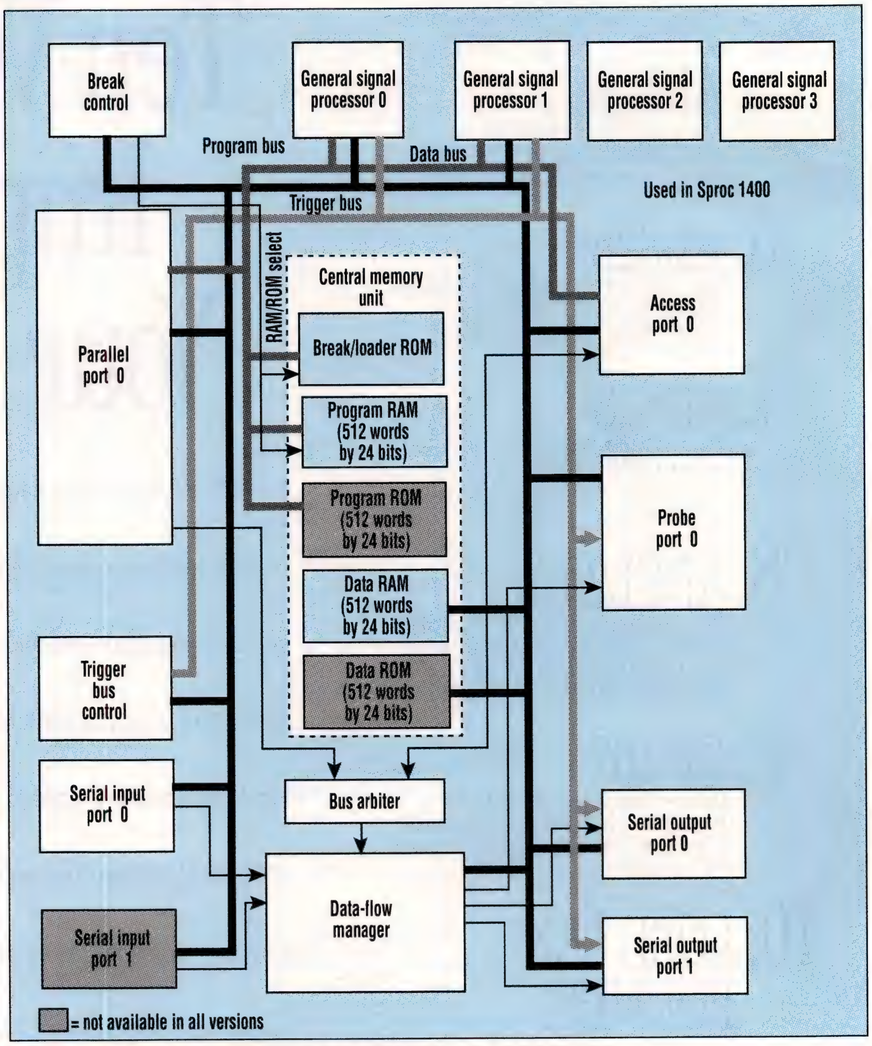
PARALLEL ROUTE

If one processor on a chip can do a credible job of handling audio, then multiple processors should be even more proficient. That's the logic Star Semiconductor Corp. used to develop its Sproc family of 24-bit parallel processors. The first implementation, the Sproc-1400, features a multiprocessor architecture optimized for real-time performance that can handle 250-kHz real-time signal bandwidths when clocked at a frequency of 50 MHz.

At the heart of the chip lies a shared central memory unit (CMU) surrounded by four independent general signal processors (GSPs). The shared memory consists of 1024 words (24 bits wide) of RAM for data storage, and a similar-sized RAM for code storage *(Fig. 2)*.

On some variants of the processor, the program and data RAMs are reduced to 512 words each. In addition, 512 words of ROM are substituted for each block once the program is defined.

To keep the multiple processors busy, four serial ports and a 24-bit (8/16/24-bit selectable) parallel port are integrated in the silicon. They let



2. A MULTIPLE-BLOCK CENTRAL MEMORY consisting of four 512-blocks of RAM is used by the two or four general-signal-processor cores and the serial and parallel ports on the Sproc-1200 or 1400 chips from Star Semiconductor. Each clock cycle is actually time-sliced into five subcycles, and the Sproc chip executes one instruction each subcycle—one for each of the four GSPs and one for an I/O operation (Sproc-1400).

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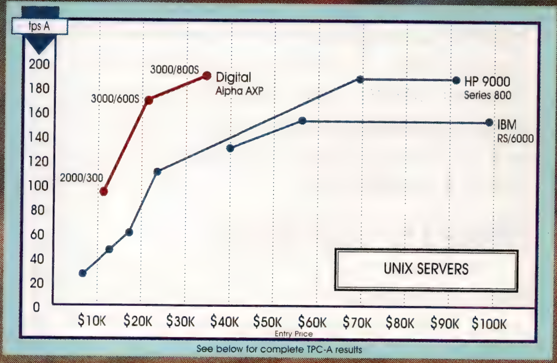

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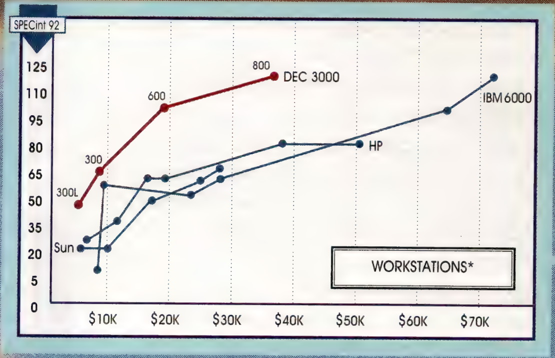

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CIRCLE 231 FOR U.S. RESPONSE

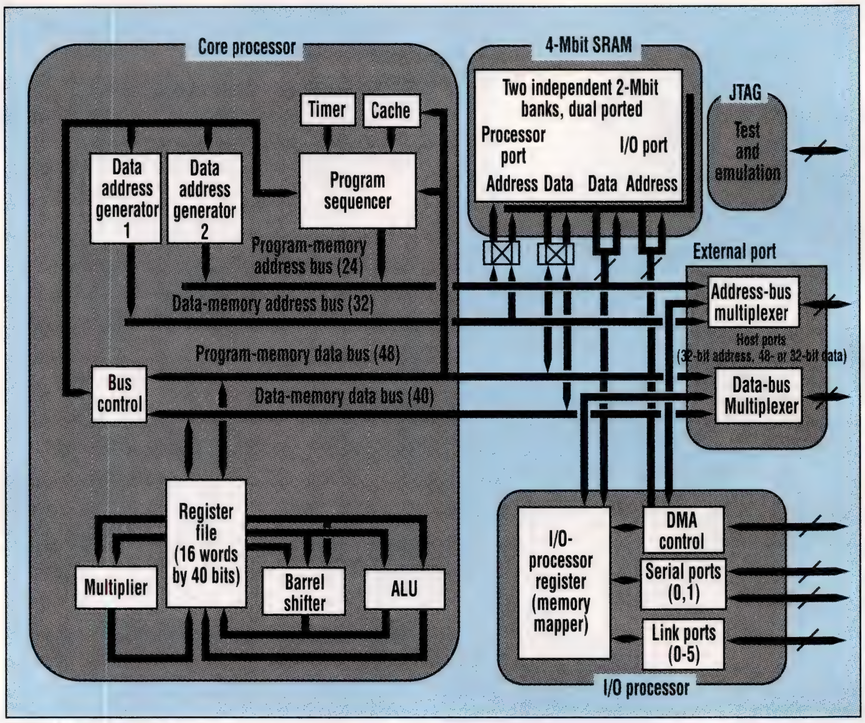
CIRCLE 232 FOR RESPONSE OUTSIDE THE U.S.

data flow into and out of the on-chip memory, as well as tie into additional DSP chips or other support circuits. A small boot ROM (512 words by 24 bits) lets the Sproc run without requiring a host processor to download instructions. Furthermore, designers can directly view signals on the chip at various points in the processing flow using a novel on-chip signal probe for diagnostics.

WIDE DYNAMIC RANGE

The 24-bit word width gives the chip a dynamic range of 144 dB—wide enough to handle over 95% of all signal-processing applications. In an example using just three of the four GSP blocks, an application that involves detecting 48 channels of dual-tone multifrequency (DTMF) telephone-tone signaling can be done with one Sproc-1400. The same chip could also decode 24 channels as well as use the first harmonics for voice discrimination. For slightly lower performance applications, the company just released a dual-GSP version of the chip—the Sproc-1200.

The Sproc-1400's central memory architecture allows concurrent signal processing by allocating each processor a time-slice of a five-cycle period (the fifth period is used for I/O operations). Each serial port on the chip can be configured for 8-, 12-, 16-, or 24-bit word lengths and has an I/O bandwidth of 715 ksamples/s. The parallel port has a bandwidth of 9 Mbytes/s and can be configured for 8-, 16-, or 24-bit transfers. By using a time-slicing scheme, the on-chip processors interact predictably, permitting tasks to be allocated across many processors. Furthermore, because task scheduling is simplified, it can accommodate many asynchronous signal streams.



3. PACKING the largest SRAM of any DSP chip, the just-released ADSP-21060 from Analog Devices employs what the company calls a Super Harvard architecture. The processor core has separate program and data address generators and dual data paths, one for instructions and one for data. This allows for simultaneous data and instruction fetches. At 40 MHz, the processor delivers a peak throughput of 40 MIPS and 120 MFLOPS.

As seen in the Zoran integer processor, the FFT is a key aspect of many multimedia audio applications, as well as a number of other different applications. The function is so popular, in fact, that several companies have created dedicated chips that act solely as very fast FFT engines. One such chip, the LH9124L, and its companion address genera-

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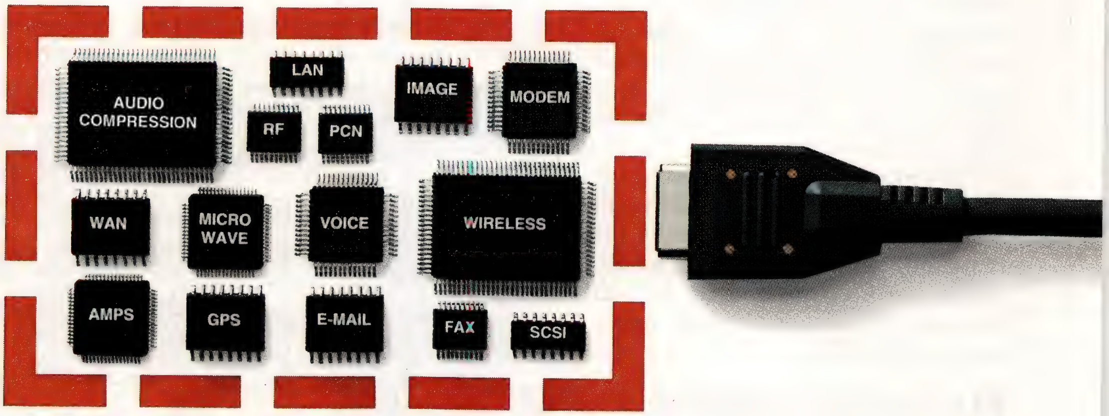

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tor, the LH9320L, developed by Sharp Electronics Corp., Camas, Wash., employs 24-bit data paths. When it's clocked at 25 MHz (the low-power version), it can execute a 1-kpoint complex FFT in just 129 ms—about one-sixth the time required by the 20-bit Zoran chip—while consuming about 3 W (for the two-chip set). A higher-performance version that operates at 40 MHz trims the FFT time to just 80.7 ms. But to get the latter speed, the chip's designers paid a price—the power consumption increases to about 6 W for the two FFT chips.

The dedicated architecture of Sharp's chip can handle data widths from 8 to 24 bits (real or complex) and moves that data around over four bidirectional and two unidirectional 24-bit-wide buses. Special on-chip resources, such as 60-bit accumulators and no-overhead indexed padding and filling of arrays, keeps internally generated roundoff noise to a minimum while ensuring that the on-chip data memory stays full. To simplify the designer's programming efforts, Sharp's programmers have already included on-chip routines for real and complex radix-2, radix-4, and radix-16 operations, as well as real and complex FIR filter operations—all in ROM.

FLOATING-POINT'S RANGE

Although integer DSPs are more popular than their floating-point cousins by a significant margin due to their lower cost, there are many applications that require the dynamic range that only floating-point DSP chips can provide. Early floating-point versions tried to economize on-chip area by employing precision levels of 18, 22, and other word sizes. However, to ease programming and the transfer of algorithms and coefficients from large computers typically used for development, most companies have now "standardized" on 32-bit single-precision floating-point DSP chips when wide dynamic ranges are needed.

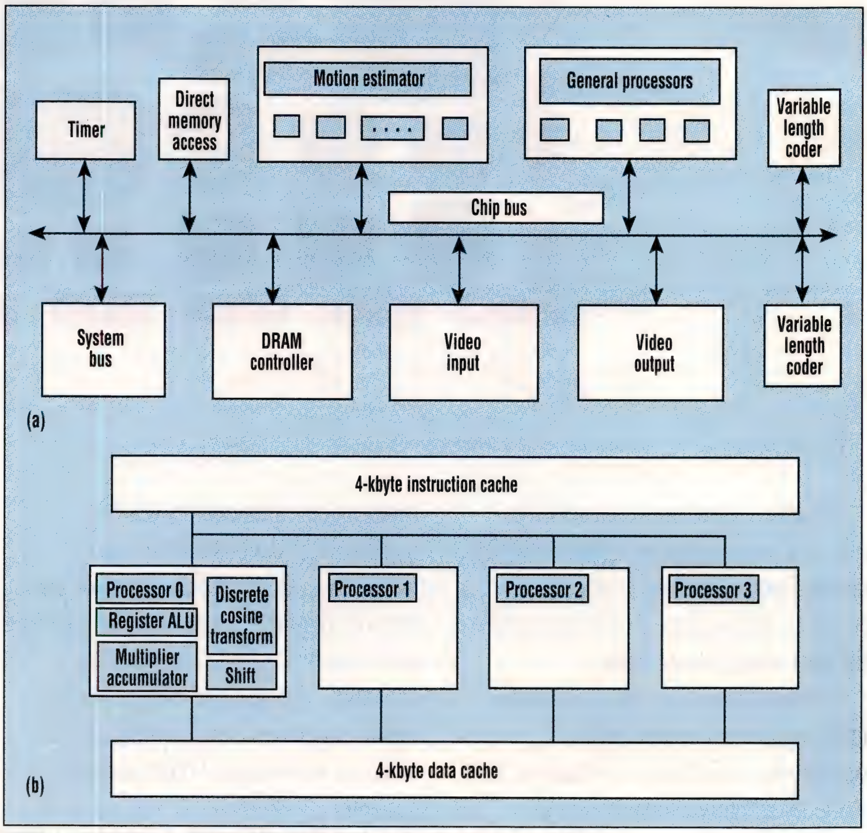
Designers at AT&T Microelectronics recently released an optimized version of the company's DSP3210 floating-point chip, the DSP3207, to handle a wide range of multimedia sound and data-communications applications. Intended to perform real-time processing of multimedia sound and high-speed modem applications, the chip can run at a top speed of 66 MHz and executes each instruction in just 60 ns. To improve performance over the DSP3210 chip, the I/O functions were repartitioned and separated from the core DSP functions.

With DSP chips being designed into many battery-powered portable systems, the issue of low-power dissipation is taking on greater importance. As a result, designers of DSP ICs are adding power-conserving features and optimizing their chips for 5- and 3.3-V operation. For example, AT&T's DSP3207 programmable DSP chip is now available in both 5- and 3.3-V versions. It incorporates a power-down mode that trims power much below the levels possible with the DSP3210 (less than 30 mW at 3.3 V), and an even lower power mode that basically shuts the chip down by gating off the clock signal (less than 3 mW at 3.3 V).

SUPPORT TOOLS

To support the chip, the company also released an upgrade to its VCOS real-time multitasking operating system (version 1.1). By running the applications on top of VCOS, the high throughput of the DSP3207 floating-point chip lets the circuit play back audio while handling a second function, such as modem data transmission, in the background.

Other companies see the low-power market as very attractive. For instance, a low-power version of TI's TMS320C31, the TMS320LC31, was released last quarter. The 32-bit floating-point DSP chip delivers 33 MFLOPS and can run at 3.3 V. Like AT&T, designers at TI incorporated two power-savings modes: one slows the processor; the other stops the



4. WITH A THROUGHPUT OF OVER 2.4 GOPS, the CL4000 single-chip image-compression/expansion processor, designed by C-Cube Microsystems, employs a central bus over which all internal processor sub-units transfer their data. The two key blocks on the chip are the motion estimator, which runs at about 2000 MOPS, and the general-purpose processor section that runs at about 240 MOPS (a). The general-purpose block actually contains four 32-bit CPU cores, each of which has access to a shared 4 kbytes of both instruction cache and data cache (b).

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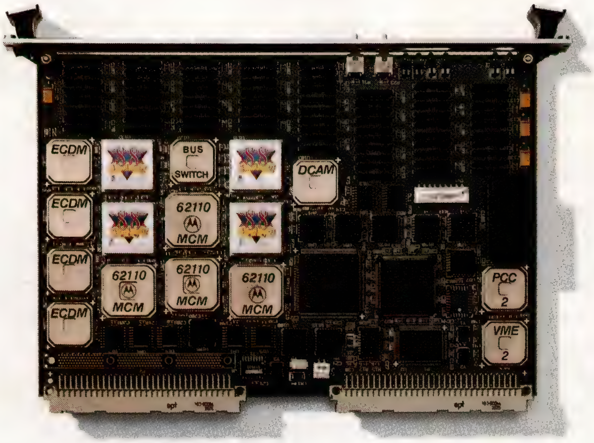

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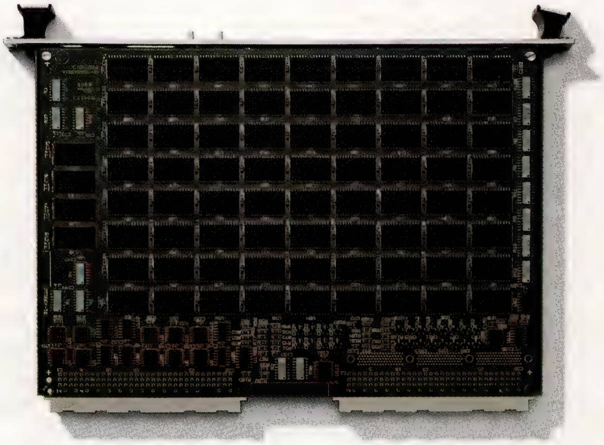

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chip but maintains the memory contents. The low-power modes are important if the chips are to be used in portable-system applications. In addition to the low-power version, a higher-speed grade of the 320C31 that runs at 50 MHz (50 MFLOPS) was also unveiled last quarter.

Analog Devices, which already offers a 32-bit floating-point DSP, just upped the ante by extending its Harvard architecture floating-point DSP family into the realm of what it dubs a "Super" Harvard architecture. The result was the ADSP-21060, which can execute 40 MIPS and 120 MFLOPS (peak)—80 MFLOPS (sustained). Not only does the circuit offer the highest floating-point throughput, but it has the largest amount of on-chip dual-ported static RAM—4 Mbits. Thus, it can hold the entire vector set for a complex algorithm such as a complex FFT *(Fig. 3)*.

Even with 4 Mbits of RAM on-chip, data must be able to transfer into or out of the memory very quickly. To that end, the circuit's designers included a ten-channel direct-memory-access controller that oversees transfers on six special link ports, two standard serial ports, and other interfaces. In addition, the circuit includes special control lines that allow the chip to be employed in multiprocessor arrays.

Design tools used to create appli-

RISC/DSP CHIP COMPARISON

	Texas Instruments	Motorola	Analog Devices	Intel
	TMS320C40	DSP96002	ADSP21020	i860
Clock frequency, MHz	50	33	33	40
Throughput, MFLOPS	50	50	50	80
Complex 1-k FFT (radix-2), μs	1545	1255	853	1024
Complex 1-k FIR, μs	NA	263	NA	102
Real FIR (80-tap), μs	3.48	5.52	3.36	NA
Device throughput, Mbytes/s	320	NA	NA	160

Notes: NA = not available; MFLOPS = millions of floating-point operations per second; FFT = fast Fourier transform; FIR = finite impulse response. Most of above chips are available with higher clock rates.

DSP ICs, PARALLELISM, AND NEURAL NETWORKS

The digital signal processor is an ideal engine for the emulation of artificial neural networks. All DSP ICs can perform the vector-inner-product operation, which is dominant in neural-network computations. In addition, all inexpensive DSP ICs can do fixed-point arithmetic, also common operations in neural networks. Consequently, when implementing artificial neural networks, these small fixed-point processors are ideal for implementing compact network solutions. For example, the complex, nonlinear problems associated with back propagation—the most dominant and very compact neural-network algorithm—can be solved with inexpensive hardware.

Neural networks are highly parallel and can therefore take advantage of the inherent parallelism of neural models. The two major approaches involved in building parallel computers are MIMD (multiple-instruction, multiple-data) and SIMD (single-instruction, multiple data). In the MIMD scheme, each data processor has its own program storage and sequencing. Typically, processors cooperate loosely by synchronizing their programs at certain points in the computations.

A MIMD approach would thus consist of several independently programmed DSP chips cooperating together to solve a single problem. A number of DSP IC manufacturers have announced chips or plans for their manufacture that contain more than one DSP engine per chip. Also being worked on are special interprocessor communication interfaces for tying those processor chips together to form large arrays.

In SIMD approaches, sometimes referred to as data-parallel computing, a single program-storage-and-sequencing facility issues the same instruction sequence to all processors. The processors are also tightly coupled so that each executes the same instruction during a clock cycle. A SIMD machine is easier to program than a MIMD system, but SIMD architectures aren't suitable for all general-purpose computing applications. However, many specific applications, such as image and signal processing, pattern recognition, and neural-network emulation, lend themselves very well to the use of SIMD approaches.

One example of a SIMD DSP implementation for neural network applications is the CNAPS (connected network of adaptive processors) developed by Adaptive Solutions. By having a single, shared-instruction sequence and control capability, each data processor can be made very small because the control and sequencer need only be integrated once on the chip.

In the CNAPS chip, many fixed-point limited-precision processors are implemented along with redundant units (to improve chip yield due to the fairly large-area chip). The resulting chip consists of 64 active 16-bit processors, each with 4 kbytes of memory, which can all be clocked at 25 MHz. The resulting throughput hits a peak rate of 1.6 billion multiply-accumulates per second, which is a respectable amount of horsepower to handle various image, signal, and neural-network processing applications.

Contributed by Dr. Dan Hammerstrom, founder and chief technical officer, Adaptive Solutions Inc., Beaverton, Ore.

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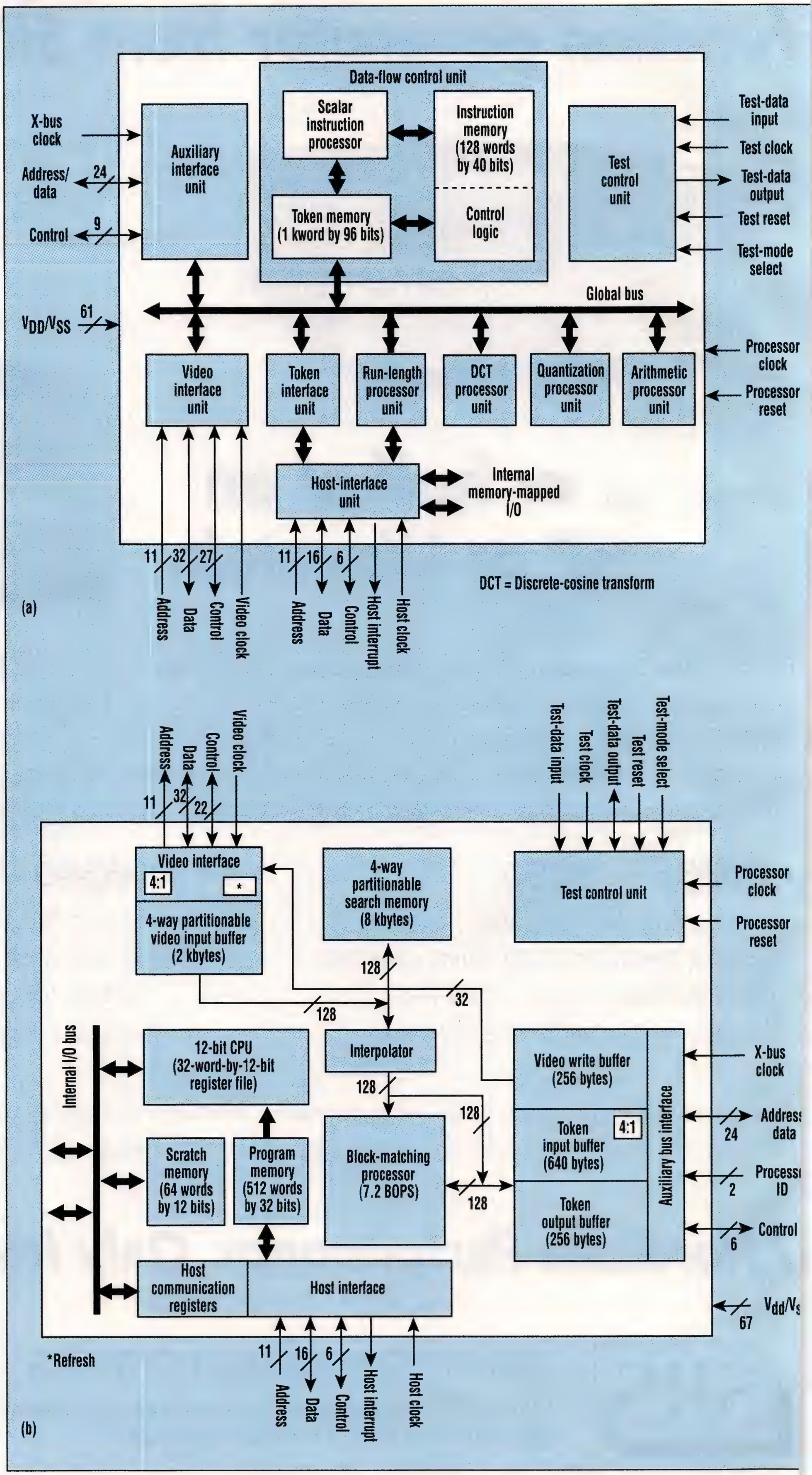
cation-specific ICs are also being applied to moderate-performance DSP cores, such as the Pine DSP core developed by DSP Semiconductors Inc. These DSP cores are now part of library functions to which support cells like analog-to-digital and digital-to-analog converters (ADCs and DACs), blocks of RAM or ROM, and other functions can be added.

Companies such as Silicon Systems Inc., which recently licensed the core from DSP Semiconductors, can take the basic DSP core and surround it with market-specific sets of resources—codecs or modems for the communications market, counter-timers and pulse-width modulators for the control market, high-speed floating-point units for the 3D graphics market, etc. Or, designers can create their own custom digital signal processor by using a DSP core and adding their application-specific peripherals and memory to form a single-chip solution.

More complex tasks, such as real-time image compression for video conferencing, multimedia, and upcoming high-definition television (HDTV), require billions of operations per second. General-purpose microprocessor-like DSP chips with throughputs of up to 50



5. THE IMAGE-compression coprocessor from array Microsystems. contains multiple processors. The device controls all operations with a scalar instruction processor that possesses its own program and token memory (a). A 96-bit-wide internal bus allows data movement between all of the subprocessor blocks at 400 Mbytes/s. At the heart of the motion-estimation coprocessor, which supplements the ICC to perform image encoding, is the block-matching processor that performs over 7 GOPS while concurrent operations take place on the video input buffer and the auxiliary bus interface (b).

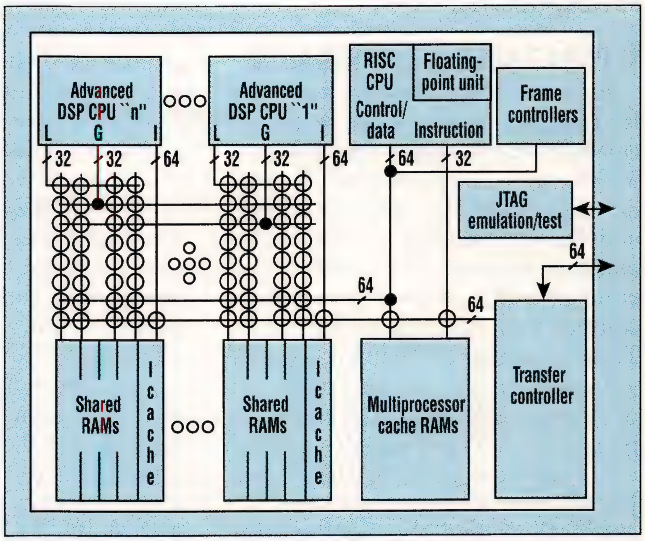
million instructions/s can't deliver the high-performance required by these applications, which typically have signal frequencies in the tens of megahertz. Such high signal speeds, require processors that can execute several gigaoperations per second.

To achieve those speeds, DSP IC designers are exploring advanced algorithms and parallel-processing schemes on both general-purpose and dedicated chips. For example, the latest round of multimedia support chips that perform JPEG or MPEG image compression or expansion are implemented with a dedicated architecture, optimized for the algorithms that the JPEG or MPEG functions require. Such chips are now available from C-Cube Microsystems, Integrated Information Technology, LSI Logic, SGS-Thomson, and many others.

C-Cube's CL4000 DSP IC, for example, can perform real-time MPEG encoding or decoding of 352-by-240-pixel images at up to 30 frames/s (or 320 by 288 pixels at 25 frames/s). It can also act as a Px64 full-duplex codec for 352-by-288-pixel images at up to 15 frames/s, as well as perform JPEG image compression or decompression (ELECTRONIC DESIGN, *Oct. 1, 1993, p. 123)*. More basic functions also possess great speed—an 8-by-8-element discrete cosine transform (DCT) and quantization operation needs just 200 clocks (at 16.5 ns/clock), while a motion-sense estimation on two 16-by-16-pixel blocks requires just 70 clocks.

Furthermore, multiple CL4000s can be employed in unison to encode even larger, high-resolution images—720-by-480 pixels at 30 frames/s. With Px64 encoding (also referred to as H.261), the codec can perform quarter compressed-image-file (CIF) and full-CIF image encoding and decoding, as well as half-duplex encoding (CIF with a 15-Hz clock) and half-duplex decoding for compressed image files with frame rates of 30 and 10 Hz, respectively.

The CL4000's 1.2 million transistors are spread among different independently controlled computational blocks that are tied together by a common internal bus *(Fig. 4a)*. To run the computations with overhead to spare, the chip's internal clock cycles at 60 MHz. The system throughput gets its first contribution of 240 million operations per second (MOPS) from a general-purpose compute engine composed of four identical 32-bit subprocessors *(Fig. 4b)*. Those subprocessors are organized as a simple array processor employing a single-instruction-multiple-data (SIMD) architecture. The four processors in the compute engine share 4 kbytes each of instruction cache and data cache.



6. A PARALLEL-PROCESSING architecture that uses a crossbar shared memory is featured on the MVP chip currently under development at Texas Instruments. The IC will contain multiple DSP CPU cores, a master RISC processor with floating-point coprocessor, and multiple shared blocks of SRAM. Each DSP core will use 64-bit-wide instructions, and the 32-bit RISC processor will employ a 64-bit-wide data bus that pulls in two 32-bit data words every bus cycle. The RISC processor's instructions are 32 bits wide.

One way of minimizing the amount of image data that must be transmitted is to send only the motion differences between one frame and the next. However, a tremendous amount of processing power is required to extract the motion from a large number of pixels. To do that job, designers at C-Cube included a 2000-MOPS motion-estimator block that contains 16 subprocessors and some control logic. The subprocessors operate as a SIMD parallel processor, and are arranged in a four-by-four matrix (to handle 16 pixels at a time). The estimator, which searches for half-pixel motion vectors, features both a programmable search range and a programmable block size. As a result, this allows the user to optimize the search and computation algorithms.

The rest of the chip contains a 50-MOPS video interface unit that handles all video data transfers, both a variable-length encoder and decoder, and an 80-Mbyte/s DRAM controller (for image and storage) with a DMA controller. The video-interface blocks give designers the option to interpolate output video data, or use the ports on those blocks as high-speed data ports. Moreover, a seven-tap decimation filter is available to preprocess the input video pixels is available.

Also targeted at multimedia video, the Vision Processor designed by Integrated Information Technology uses a 64-bit internal architecture for video-signal processing based on DCTs. It can execute JPEG, MPEG, and CCITT H.261 (Px64) video compression/decompression algorithms. The device's RISC-like compute engine executes microcoded instructions that would be incorporated into an on-chip ROM. Catalog versions of the chip, with predefined microcode, are available. Designers can also work with IIT to develop custom algorithms that can be integrated in the on-chip ROM.

A superset of the Vision Processor, the VCP, was unveiled last month. It replaces both the Vision Controller (a support chip for the Vision Processor) and the Vision Processor itself, adding programmable video pre- and post-processing and communications features. The VCP can thus be used in video telephones, desktop video platforms, and other applications that need real-time video compression.

UPGRADABLE PERFORMANCE

By dedicating silicon for a particular function, just the right resources can be integrated on a chip, minimizing chip area and silicon cost. However, that limits the chip's flexibility and leaves both the manufacturer and user in the lurch if a better algorithm or a different set of on-chip resources can improve performance. Thus, a number of companies are developing programmable parallel-processing DSP chips that can easily be modified. Two examples of such architectures include the VideoFLOW chip set created by array Microsystems and the forthcoming MVP programmable parallel processor currently being developed by Texas Instruments.

Because algorithms are continually enhanced, locking in the hardware or accepting lower performance may both be intolerable options. To deal with this difficult dilemma, designers at array Microsystems crafted an image-processing solution, which is in part funded and supported by Samsung Electronics Co., Seoul, South Korea.

The initial VideoFLOW architecture consists of two CMOS chips: the main device is the image-compression coprocessor (ICC); the companion chip is the motion-estimation coprocessor (MEC). In addition to defining the silicon, array Microsystems has worked with SofTech Corp., Waltham, Mass., which created the VideoFLOW software development tools (including a flow-graph editor, an assembler and linker, and an ICC/MEC simulator).

The ICC combines limited programmability and high-performance dedicated processing blocks. When the two chips are used, the 50-MHz chip set will tackle video compression/decompression applications based on CCITT/ISO standards with a resolution of up to 4096-by-4096 8-bit pixels per component. For decompression only, just the ICC chip is required. In a typical system, the ICC ties into either a DRAM- or VRAM-based video memory and employs two more buses.

One bus ties directly to the MEC; the other bus ties to both the MEC chip and to another processor. That processor can be either a general-purpose CPU (such as a RISC CPU), or a programmable DSP chip. The MEC circuit also has a third bus that ties into a DRAM-based video-memory subsystem which supplies data directly to the MEC. The resulting subsystem requires little or no glue logic for the DRAM or VRAM interface, thus greatly simplifying the overall system design.

The core DSP engine in the ICC chip performs over one billion operations per second (1 BOPS) and employs about 1.8 million transistors to do the job *(Fig. 5a)*. Implemented in a highly modular, token-passing architecture, the ICC can easily be modified to add new functions or remove unwanted blocks. This allowed array Microsystems to quickly bring application-optimized versions to market, or customers could create their own custom version. The companion MEC is used when MPEG and Px64 motion-compensated encoding must be performed. It executes about 7 BOPS by using approximately 1 million transistors *(Fig. 5b)*.

The chips can handle motion video at 30 frames/s and perform JPEG encoding or decoding for CCIR-601 720-by-480-pixel images. The MEC can encode and decode all standards, doing so simultaneously for Px64 and JPEG standards. For Px64 algorithms, it performs single-encode/two-decode operations on CIF (Common Interface Format) images (352-by-288-pixel), or single-encode/seven-decode operations on QCIF (quarter CIF 176-by-144-pixel images).

MPEG encoding can be done at 30 frames/s for 352-by-240-pixel SIF (source input format) images, and MPEG decoding for NTSC (National Television System Committee) or two SIF images. The circuits also support the full displacement range of MPEG motion vectors—half-pixel motion vector resolution and multiple B frames per P frame for both encoding and decoding. Even higher performance can be achieved if multiple MEC chips are added to the ICC. However, the MEC is only needed in encoder applications that require motion estimation. Color-space conversion or image up/down sampling isn't performed by the chips.

Design activity by TI on its MVP chip is reaching feverish proportions since the company unveiled the first details of the parallel processor earlier this year at the IEEE Hot Chips conference at Stanford University, Stanford, Calif. The processor will incorporate multiple 32-bit integer units, a single floating-point coprocessor, and a flexible crossbar switch to interconnect the multiple processors with multiple banks of memory for the DSP CPUs. The chip also includes a separate memory block that holds both instruction and data caches for the RISC engine that oversees the entire chip's operation *(Fig. 6)*. The chip is targeted at applications that run well on parallel processors. There are no immediate plans for it to run an existing application's binary object codes that operate on the TMS320 family.

The MVP, which ranks as one of the most complex DSP chips defined to-date, packing over 3 million transistors, will employ multiple, full 32-bit DSP blocks, each with their own multiplier, splittable (on 8-bit boundaries) arithmetic and logic unit, and shift and bit-field hardware (including barrel rotation). The DSP blocks can be independently controlled and can execute their own instruction streams, thus giving the MVP a multiple-instruction/multiple-data machine architecture. Data words are 32 bits wide; however, instruction words are 64 bits wide, which allows for more internal parallel control. Thus, more can get accomplished during each cycle.

The on-chip RISC processor (optimized for C-coded algorithms) and the floating-point unit are also 32-bit engines capable of single-cycle integer or floating-point computations. The IEEE-754-compatible floating-point unit can do several operations in parallel to save precious cycle time. In one cycle, it will be able to perform a multiplication operation, an addition operation, and a 64-bit load/store operation.☐

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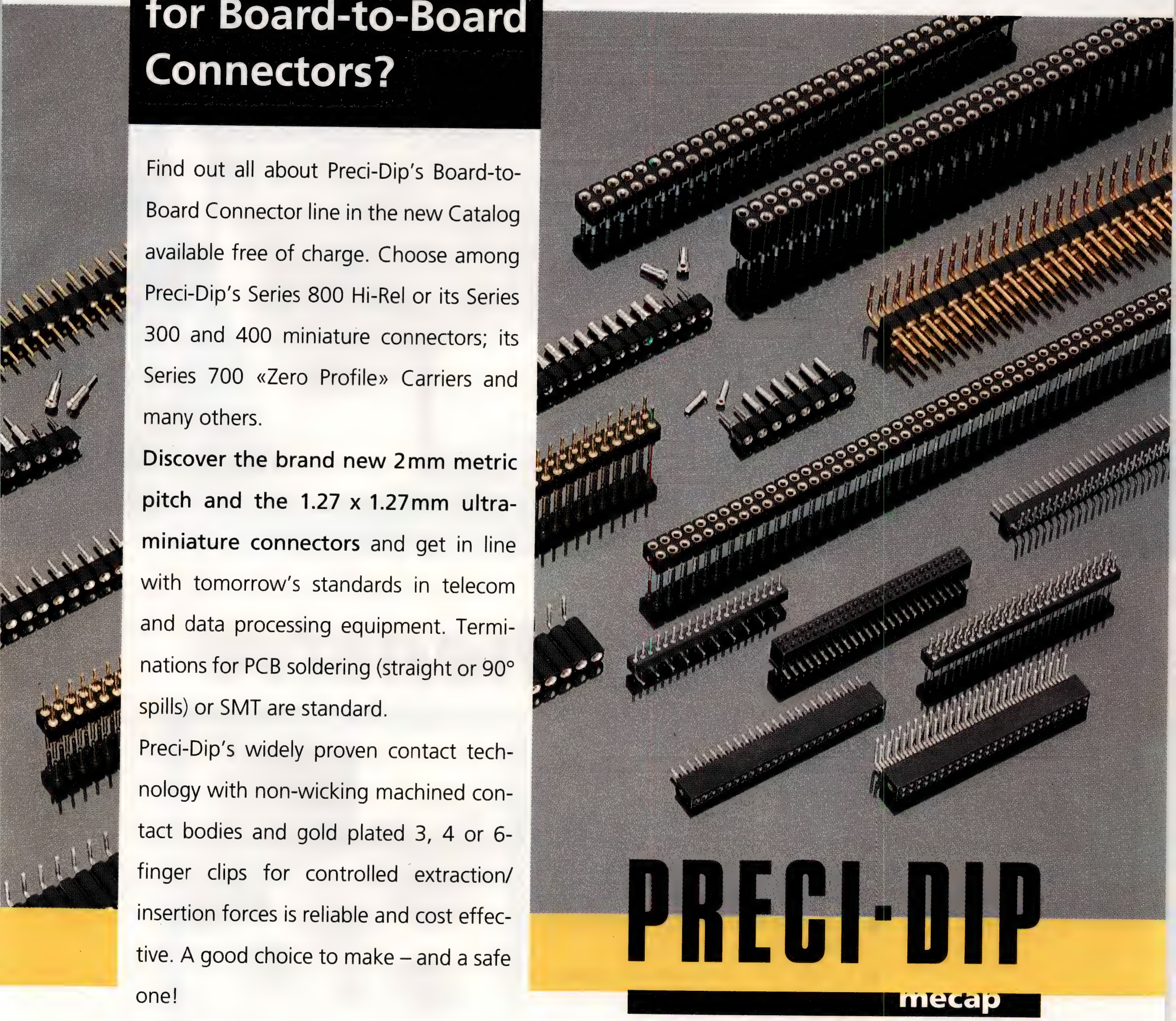

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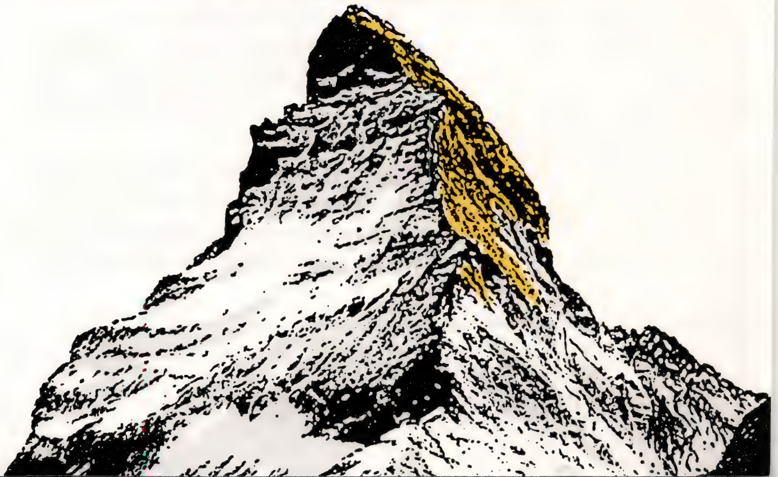

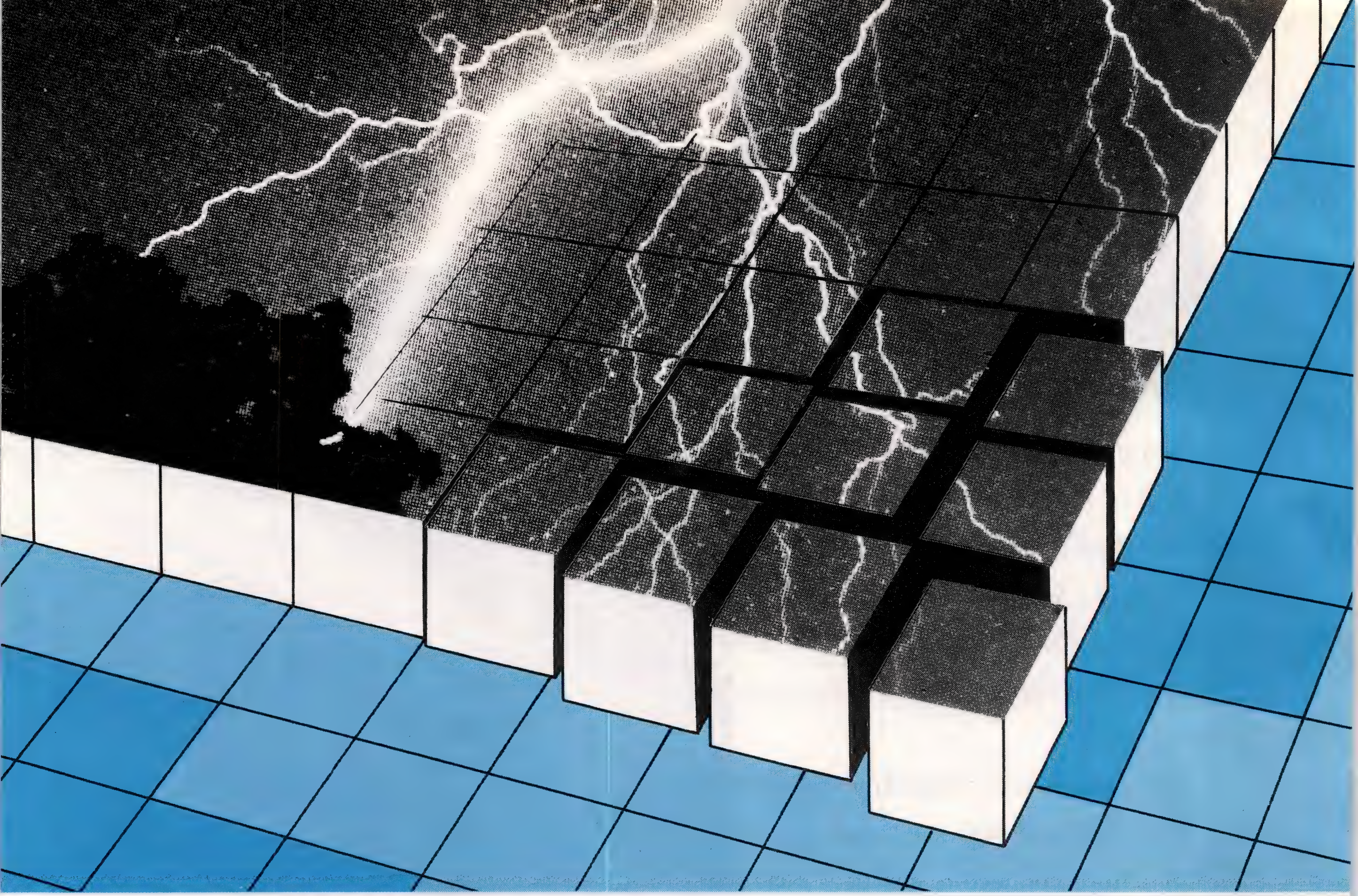

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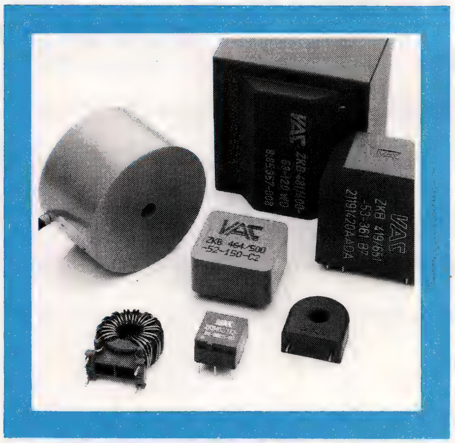

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VIRTUAL DESIGN SPEEDS EMBEDDED SYSTEMS WORK

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When you talk embedded systems, the main focus is on custom-built hardware matched with customized application software. Such a setup, though, presents developers of these systems with a special challenge: Target hardware often is unavailable until late in the project, and developers usually lack a complete set of facilities for software development and debugging.

A technique called "virtual design," however, uses a set of tools that allows development of embedded-systems software without target hardware. The "virtual development environment" is a simulation environment that offers a rapid prototyping capability for target hardware, and simulation for input and output devices. Included is a complete set of tools for the development of embedded-system software.

At the board-granularity level, a feature called "virtual target" supports a transparent interface between hardware and software I/O devices. The virtual target allows software modules to be "swapped in place" with the hardware modules, thus it has minimal effect on the application code. This article describes the basic features of the virtual development environment, along with a design example.

Two major characteristics of embedded systems are tight integration among software and hardware components, and long delays in hardware availability for software development. Tight integration makes it difficult to quickly adjust the design in one domain based on design changes in another domain.

For example, a decision to increase the number of I/O ports will usually require additional device drivers and

TABLE 1: VIRTUAL TARGET DEVELOPMENT TIME

	Design Time (Hours)	Development Time (Hours)	Test Time (Hours)	Subtotal (Hours)
Socket logic device driver	2	6	6	14
LDD test programs (target and host)	2	4	4	10
Specification file	NA	NA	NA	0.5
Total				24.5

NA = not applicable

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trigger changes in the application software. Also, the traditional sequential design process, in which software development follows hardware development, complicates the design of embedded systems.

To overcome the lack of hardware, embedded-system software developers have used hardware emulators and simulators of the target hardware's architecture. With these emulators and simulators, developers can design, develop, and verify the functionality of their software concurrently with hardware development. This approach allows some flexibility in the design of the software, but at the expense of higher design costs (the price of the emulator) and design time (the time spent developing a simulator).

Simulator development, in particular, requires substantial effort and diverse expertise, such as graphical windowing systems and a host operating system. Also, these simulators often provide only crude functionality, so applications developed with them frequently need to be re-engineered (or re-implemented) when the hardware becomes available.

HARDWARE ESSENTIAL

Therefore, developers of any software subsystem (for example, application, kernel, device drivers) must have a solid working prototype of the hardware (including the target and I/O subsystem) available, as well as other software subsystems. To solve the problem of hardware unavailability, design frameworks should have tools that allow rapid prototyping of target hardware and I/O subsystems without expensive hardware emulators and tedious simulator development.

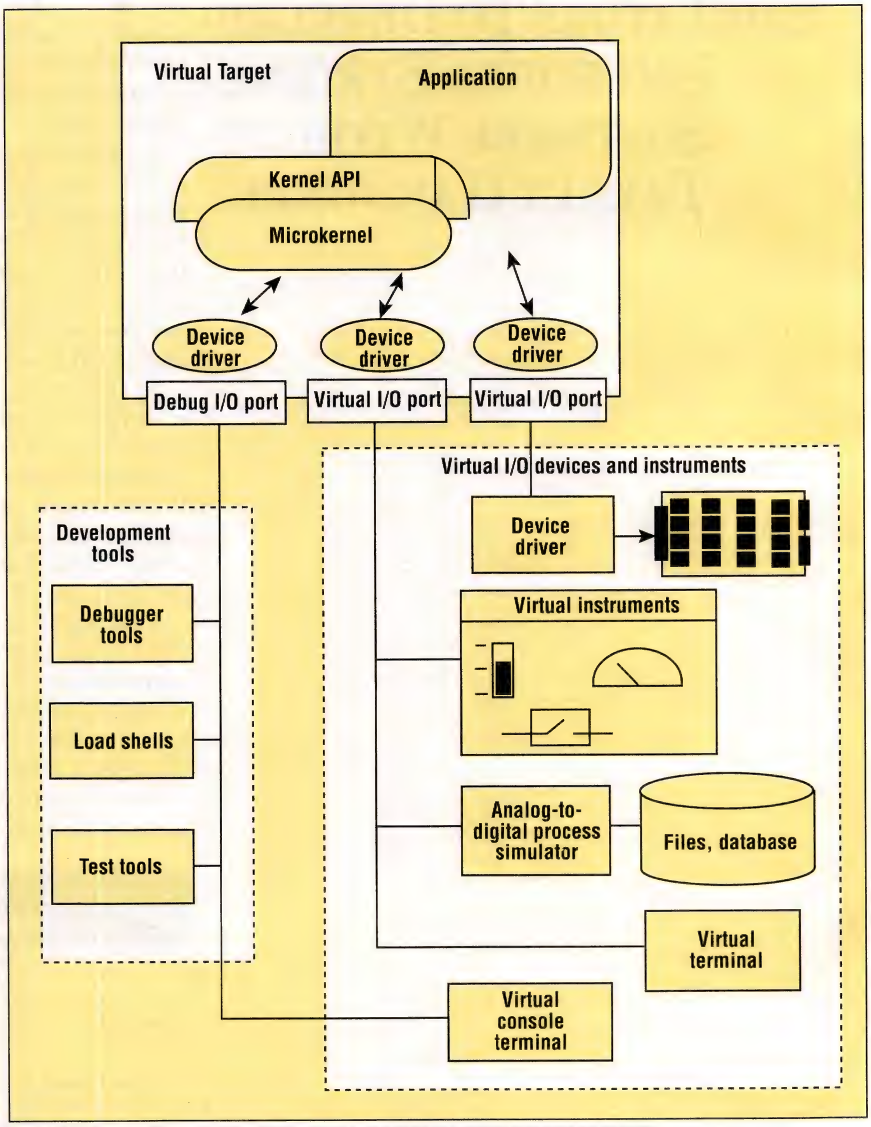
The prototypes should be at a level of abstraction that doesn't require other subsystems relying on the prototypes to change significantly when the final working subsystems are available. That is, the tools should provide an abstract model of the target resources with swap-in-place capability, so the application-software develop-debug-test process can transparently move from prototype to actual target hardware.

In this environment, only recompilation of the application software should be required. Furthermore, the development, debugging, and testing tools used in the process should not change. Such a design environment will provide a measurable improvement in designer productivity, a reduction in cost, and an increase in product quality.

A complete virtual development environment must supply a framework for specification, design, development/debugging, simulation/prototyping, and testing of embedded-system software. The environment should encompass tools and techniques that enable:

- Description of the system and its interfaces and attributes, such as performance, reliability, size, and cost
- Phased refinement and verification of the design
- Rapid prototyping to allow analysis of architecture and performance trade-offs
- Efficient testing through transparent interfaces between hardware and software components, such that a software module can be swapped in place with a hardware implementation of the same module

A virtual development environment consists of a virtual target and virtual I/O devices and instruments



1. A VIRTUAL DEVELOPMENT ENVIRONMENT creates a virtual target, which can be used to develop embedded-system software by porting key elements of the target-resident environment to a host machine. The virtual target is an abstraction of the physical target within the host machine.

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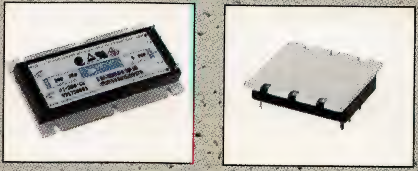

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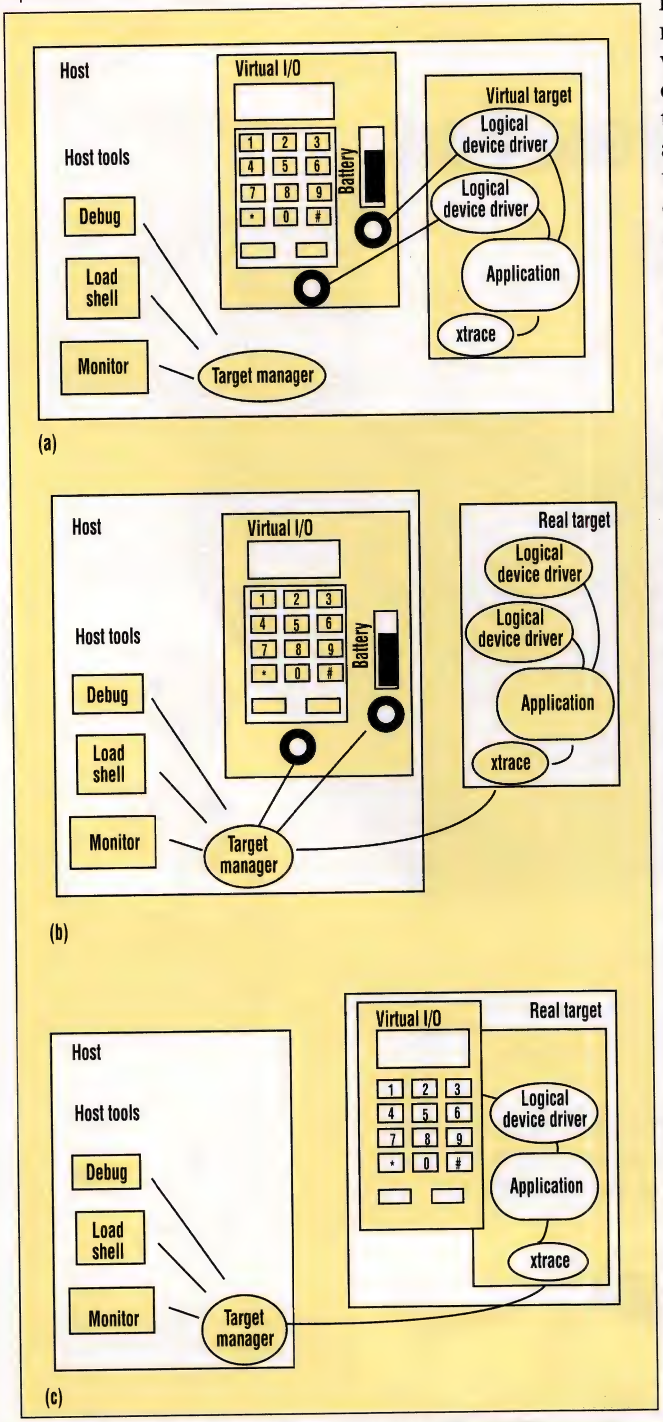
CIRCLE 237 FOR U.S. RESPONSE

CIRCLE 238 FOR RESPONSE OUTSIDE THE U.S.

(Fig. 1). The virtual target is an abstraction of the physical target within a host machine, which can be any Unix-based computer. By porting key elements of the target-resident environment to the host system, embedded-software developers can execute C language application code on the host machine.



2. THE VIRTUAL DESIGN PROCESS progresses with hardware availability, as can be seen in this example. The primary changes occur in the evolving logical device drivers (LDDs), as the project goes from no hardware available (a), to a real target available (b), to the full system ready for verification (c).

The virtual target offers an application the same operating system (OS) and I/O interface as does the real target. This means software developers can realistically debug multitasking embedded applications without target hardware, including portions of application or device driver code that interact closely with the OS or I/O interface.

The virtual target isn't a simulator. It runs application and device driver code in the context of a bare machine or a real-time executive (for example, a off-the-shelf real-time operating system or custom kernel) on the host system's processor. Software developers can configure the memory map of the virtual target, compile C application modules using native tools, link them together incrementally, and then download them to the virtual target. In addition, the virtual target can be easily configured to include different types and numbers of virtual I/O ports.

Once an application is downloaded, developers can debug the application with the same tools that will be used on the real target. If the host employs the same processor as the target, software developers can also use the virtual target to debug at the assembly level.

The main characteristics of the virtual target are:

- Support for high-level language (C and C++) code development, debugging, and testing
- Rapid prototyping of simulated target hardware
- Support for non-OS and OS applications (for example, the VRTXsa-Multi-threaded real-time kernel developed by Ready Systems)
- Multiple virtual targets on one host
- Configurable memory and virtual I/O ports (devices)
- Expandable virtual I/O ports and I/O instruments

To implement the "virtual instruments," software developers can use off-the-shelf graphical modeling packages such as DataViews (VI Corp., Northampton, Mass.), SL—GMS (SL Corp., Corte Madera, Calif.), TEA+ (NASA), and TCL/Tk (University of California at Berkeley). The main characteristics of these packages are:

- Rapid prototyping tools for I/O stimuli for use with both virtual and real targets
- Configurable virtual I/O Instrument panels
- Expandable virtual I/O Instrument panels with new custom devices

The example design-process described here demonstrates the effectiveness of the virtual target concept in the development of embedded-systems software. The technique is used for a handheld communication device or instrument, such as a cellular phone. Typically, this consists of the target board and an instrument panel, additional I/O inputs for gathering "environment" data, and usually an I/O channel for data transfer to and from other data-processing equipment (such as a remote computer system).

In the final production system, the operator interface hardware acts as a custom LCD display with a set of keys. This type of architecture is found in a number of applications, including telecommunications, transportation, power systems, and medi-

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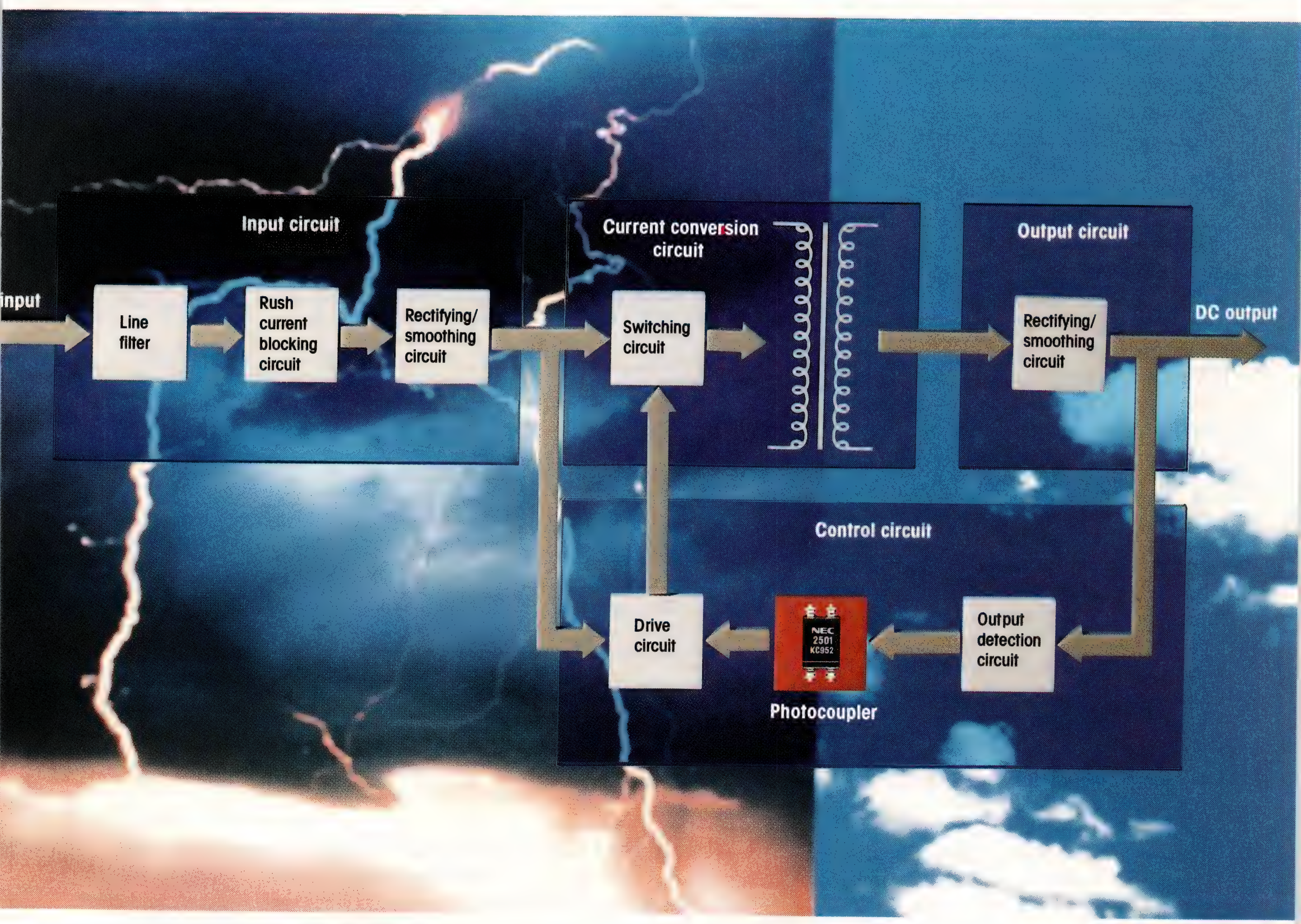

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CIRCLE 218 FOR U.S. RESPONSE

CIRCLE 219 FOR RESPONSE OUTSIDE THE U.S.

cal monitoring.

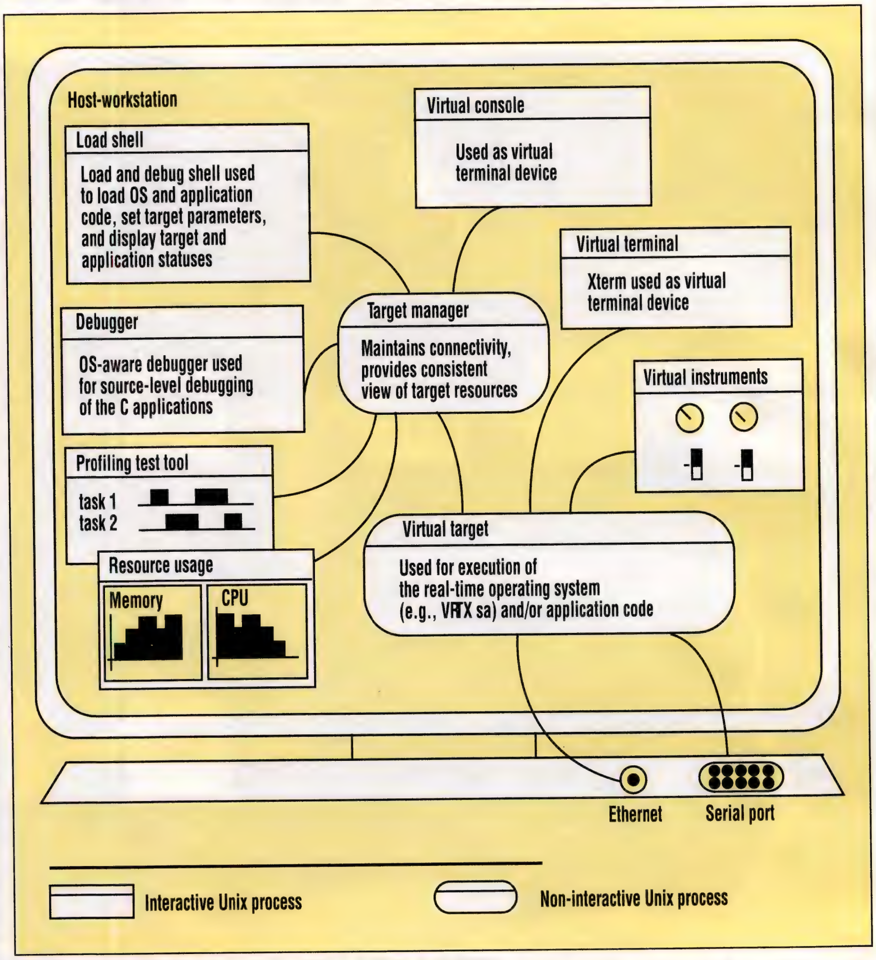
The first phase of the process is the environment used by the software developers when no hardware exists *(Fig. 2a)*. At this stage, both the computing and the display hardware are being designed and implemented. The virtual target supplies the basic CPU execution engine to serve as a prototype of the actual hardware.

The developers use an off-the-shelf virtual instrument package, such as DataViews, to simulate the instrument's actual LCD display. Note that the engineers developing the display can also use this environment to test various concepts in the display before their design is frozen.

A KEY INTERFACE

The logical device drivers (LDDs) are critical interfaces that ease the transition to actual hardware. Thus, they play a key role in the swap-in-place concept. The application accesses the simulated LCD only through the LDD defined for the display. The LDD interface remains constant, even as the process changes from driving a simulation to driving the actual display. In the virtual target environment, the LDD uses standard Unix communication facilities, typically the socket interface, to establish a connection to another process that will support the display simulation.

The programming environment for the display simulation is that of a normal Unix C program, enhanced with the virtual instrument package used to build the LCD display simulation. In addition, the display-simulation software uses the socket connection to synchronize and communicate with the logical device driver on the virtual target.


Host-workstation
Load shell
Load and debug shell used to load OS and application code, set target parameters, and display target and application statuses
Debugger
OS-aware debugger used for source-level debugging of the C applications
Profiling test tool
task 1
task 2
Resource usage
Memory
CPU
Virtual console
Used as virtual terminal device
Virtual terminal
Xterm used as virtual terminal device
Target manager
Maintains connectivity, provides consistent view of target resources
Virtual instruments
Virtual target
Used for execution of the real-time operating system (e.g., VRTX sa) and/or application code
Ethernet
Serial port
Interactive Unix process
Non-interactive Unix process

3. AT THE BOARD GRANULARITY level, the Spectra Virtual Target Environment creates a transparent interface between hardware and software I/O devices. The package uses host-resident tools to develop and debug application code on the host computer, which can be any Sun3 or Sun4. Virtual Instruments are included to supply input and output simulation.

As the hardware design progresses, the target computing hardware becomes available. The application software then moves from the virtual target to the actual target hardware. The connection from the target manager to the virtual target moves to the real target, using an external hardware link such as a serial line *(Fig. 2b)*. However, even though the underlying hardware and its connection to the tool software changes dramatically, the developers use the same toolset as that of the virtual target.

The LCD hardware is still unavailable, so the developers must continue to use the simulated display. To do so requires replacing the LDD from the virtual target with an LDD that runs on the real target. Notice that the target-resident LDD now uses the debugging channel provided through the target manager (the host-resident part of the debugging server) and xtrace (a target-resident part of the debugging server) to pass information to the display simulation.

The host-resident display-simulation software then changes its lower-level interface from the socket-based connection of the virtual target to the target-manager-based connection. But the application software never sees this change.

In the final stage, the tar-

TABLE 2: VIRTUAL INSTRUMENT DEVELOPMENT TIME

	Design Time (Hours)	Development Time (Hours)	Test Time (Hours)	Subtotal (Hours)
Customize buttons	0.5	4	0.5	5
Specification file (automatically produced)	NA	NA	NA	NA
DVserver	4	8	8	20
Total				25

NA = not applicable

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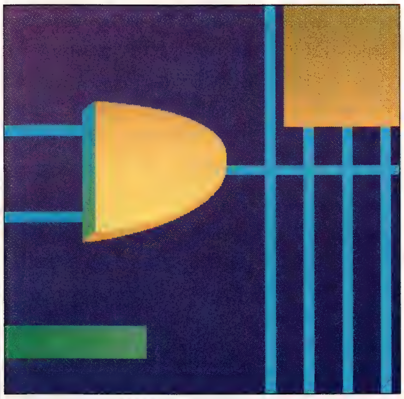

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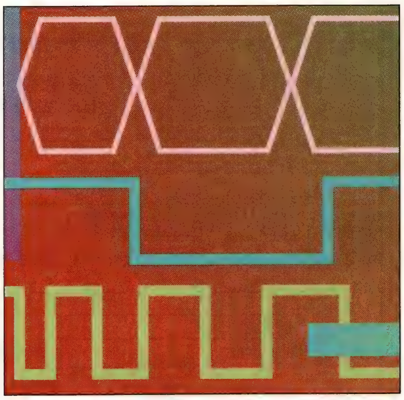

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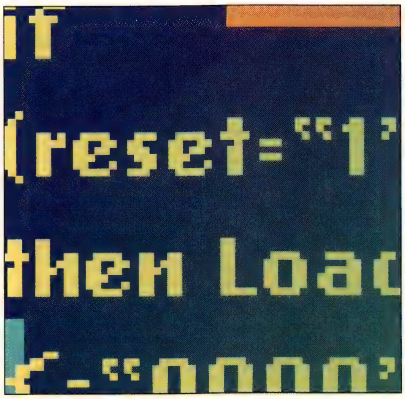

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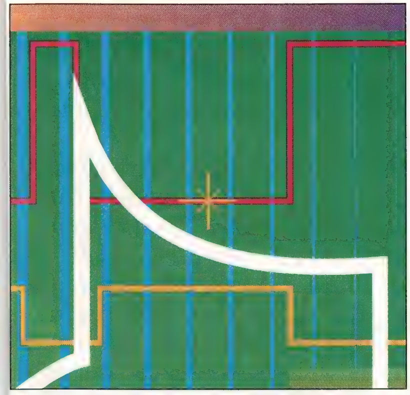

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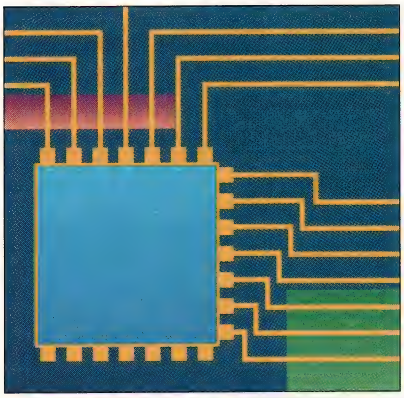

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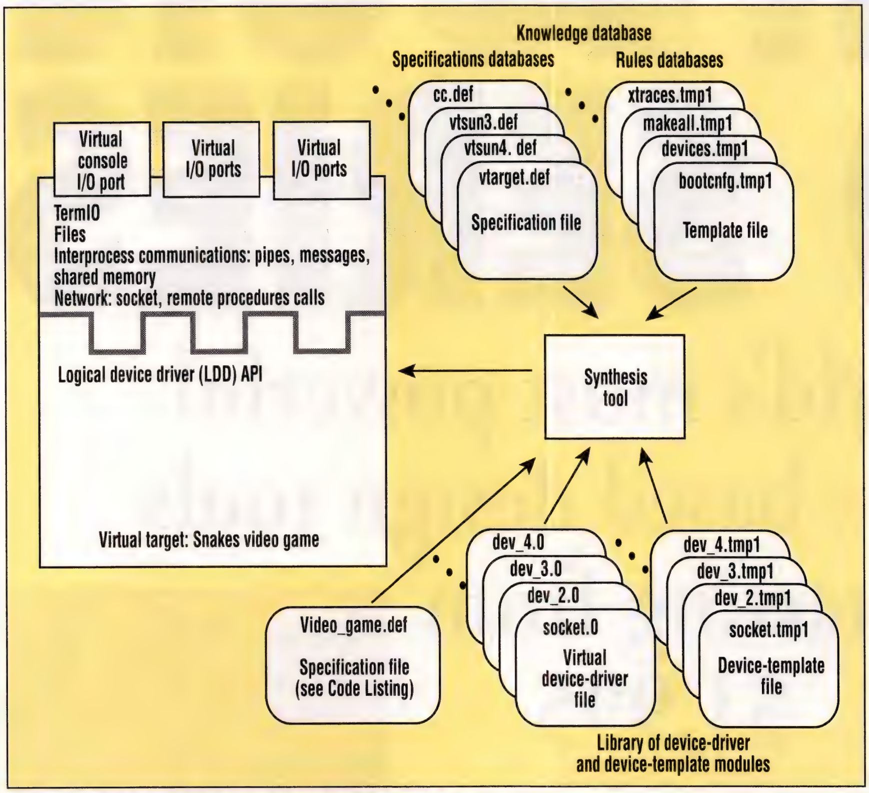
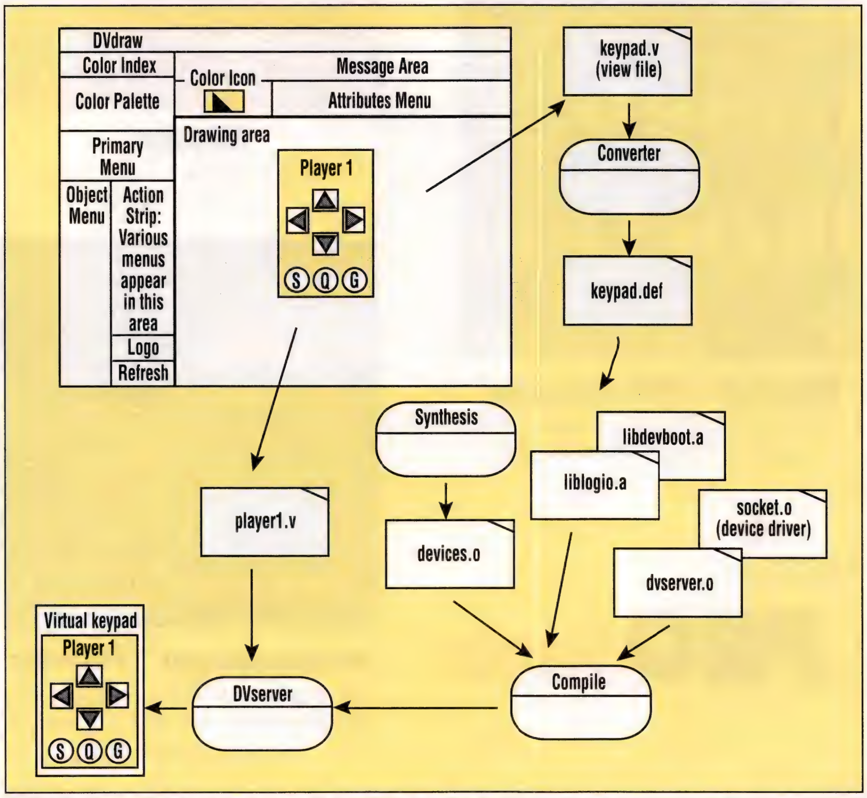
CIRCLE 213 FOR U.S. RESPONSE

CIRCLE 214 FOR RESPONSE OUTSIDE THE U.S.



4. THIS DIAGRAM ILLUSTRATES an example of the synthesis process by which a new virtual target is created. Two additional virtual I/O ports use Unix sockets.



5. TO RAPIDLY CREATE A PROTOTYPE of the virtual instruments for the example video game, Spectra relies on DVdraw, an interactive drawing editor for creating customized user-interface screens.

get hardware includes the actual LCD display hardware *(Fig. 2c)*. The LDD is now modified to drive the real LCD rather than the simulated LCD. The application software still sees the constant LDD interface and, consequently, will not change.

This example illustrates that by establishing the appropriate interfaces early in the development process, the application software can remain essentially unchanged throughout the process. As a result, the developers' confidence in the software was greatly enhanced because it had run for a larger part of the development cycle.

SUN HOSTS USED

The Spectra Virtual Target Environment (SVTE) designed by Ready Systems consists of the company's Virtual Target (VT) tool and VI Corp.'s DataViews virtual instruments package *(Fig. 3)*. As noted, the virtual target is an abstraction of the physical target within a host machine, which can be any Sun3 or Sun4 computer. VT allows developers to execute C-language application code within the context of the virtual target on the host machine. Host-resident tools help develop and debug application code on the host computer. Virtual instruments supply input and output simulation.

At the board-granularity level, SVTE creates a transparent interface between hardware and software I/O devices. The hardware abstraction layer is provided by a board support package (BSP), which consists of LDDs and logical I/O (logio) functions.

The logical device drivers consist of the generic device access functions: *logio_device_init, logio_device_read, logio_device_write, logio_device_control, logio_device_getmsg, logio_device_putmsg* and *logio_device_poll,* as well as interrupt handling support. Software (that is, the kernel, OS, application, etc.) doesn't communicate with physical devices, but rather with abstract I/O objects.

The input to a logical I/O function is a device ID that determines which physical or virtual device is affected by a logical I/O function call. From the viewpoint of the software, the in-

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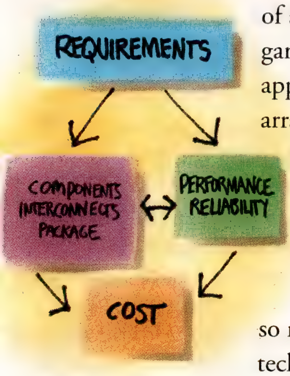

Remember, an MCM is a system comprised of the components, the interconnects and the package – all of which are selected based on your requirements for performance, reliability and affordability. The cost is the composite result of the selections made.

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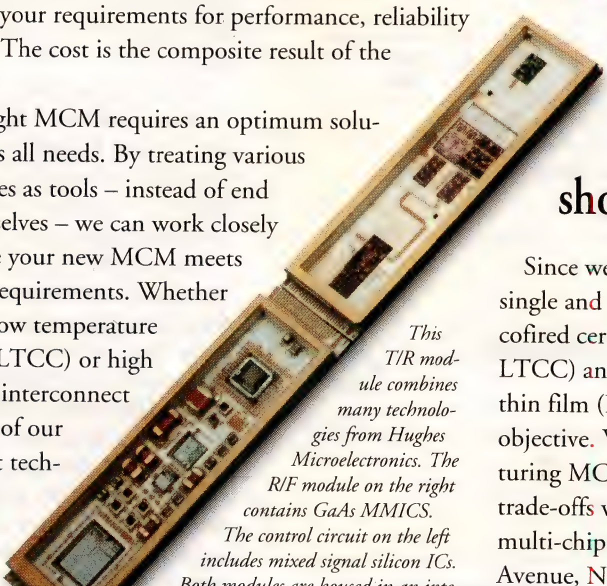


This T/R module combines many technologies from Hughes Microelectronics. The R/F module on the right contains GaAs MMICS. The control circuit on the left includes mixed signal silicon ICs. Both modules are housed in an integral LTCC substrate package.

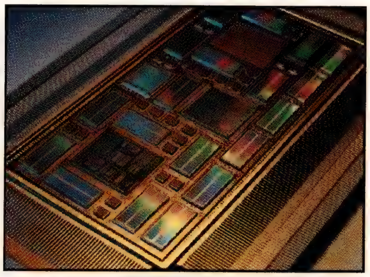
What's LTCC?

LTCC is a variant of MCM-C which fires at temperatures low enough to use noble metals such as silver or gold. It accommodates a variety of packaging needs. Extremely low profile packages are created by using cavities to hold silicon or GaAs semiconductors. Heat is dissipated by placing high power devices on thermal vias or a heat spreader attached to the back surface through a hole or cavity. By burying resistors, capacitors and inductors with a broad range of component values and tolerances, substrates/packages actually become large passive ICs.

What's HDMI?

It's a thin-film multilayer technology essential for the next generation of high-speed miniature electronics systems as used in computers, workstations and signal and data processors.

Which MCM technology should you use?



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CIRCLE 120 FOR U.S. RESPONSE **CIRCLE 121 FOR RESPONSE OUTSIDE THE U.S.**

CODE LISTING

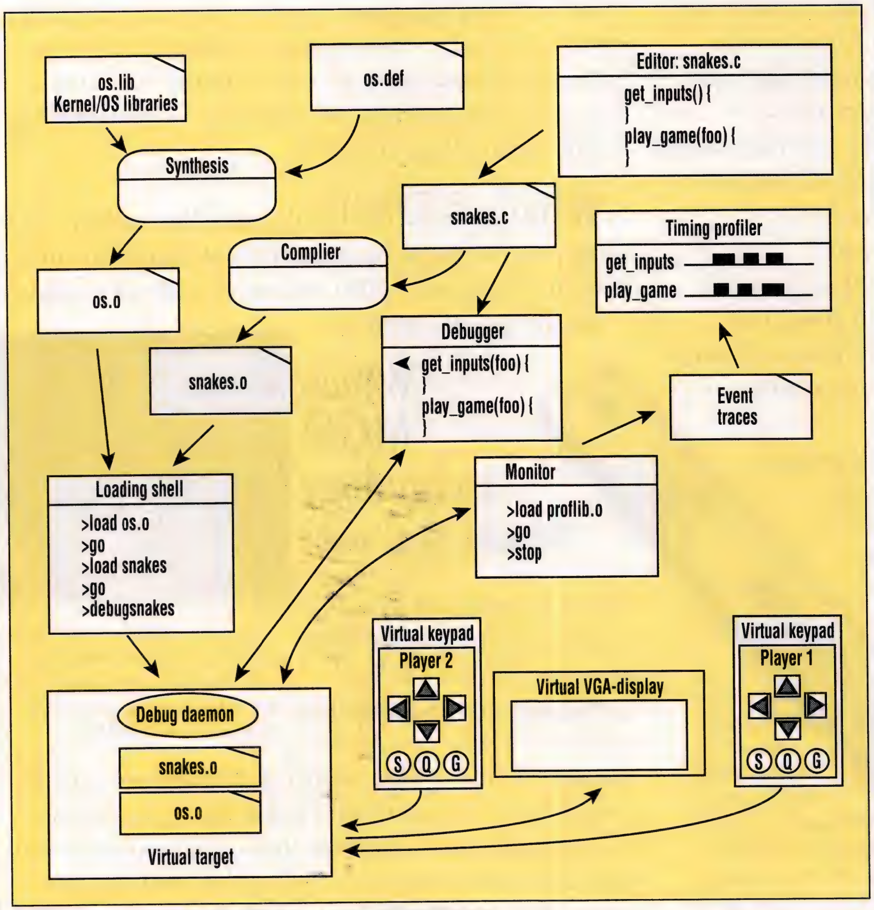
```
#include(vtarget.def)
#include(vtsun4.def)
#include(cc.def)
dev.keypad_1.type: socket
dev.keypad_2.type: socket
dev.keypad_1.name: KEYPAD_1
dev.keypad_1.method: logio_keypad_1_method
dev.keypad_2.name: KEYPAD_2
dev.keypad_2.method: logio_keypad_2_method
board.devices.usr: keypad_1, keypad_2
vtarget.objs.usr: ./socket.o
vtarget.libs.usr: /usr/lib/libc.a
board.memory: 0x000000, 0x20000, BOOTOS_MEMORY_UNUSED_HOST, 0},{0, 0x100000, BOOTOS_MEMORY_UNUSED_TARGET, 0},
```

terface to the hardware remains the same. Therefore, none of the target software, other than the BSP, addresses the underlying hardware, whether physical or virtual.

System designers can swap in place two physical targets with the same I/O capabilities without changing the application software. They can also swap in place virtual and physical targets without changing the software.

Swap-in-place capability applies not only to the targets as a whole but also to the individual I/O devices. For example, on a physical target, you can swap the physical console device (the character terminal) with the virtual console (the terminal emulator program executing on the host in the context of an X terminal). Spectra also allows logio device driver modules to be swapped in place.

Although application software is unaffected by a swap, a change in the configuration of the devices requires that the target be reconfigured. In the case of the physical target, a modified BSP must be generated. For the virtual target, a new virtual target is built.



6. THE DEBUGGING AND TESTING process for the example video game starts with development of the kernel, which is built using the synthesis tool and loaded using a loading shell. After the kernel is started, the application program is compiled, loaded, and started.

AUTOMATED SYNTHESIS

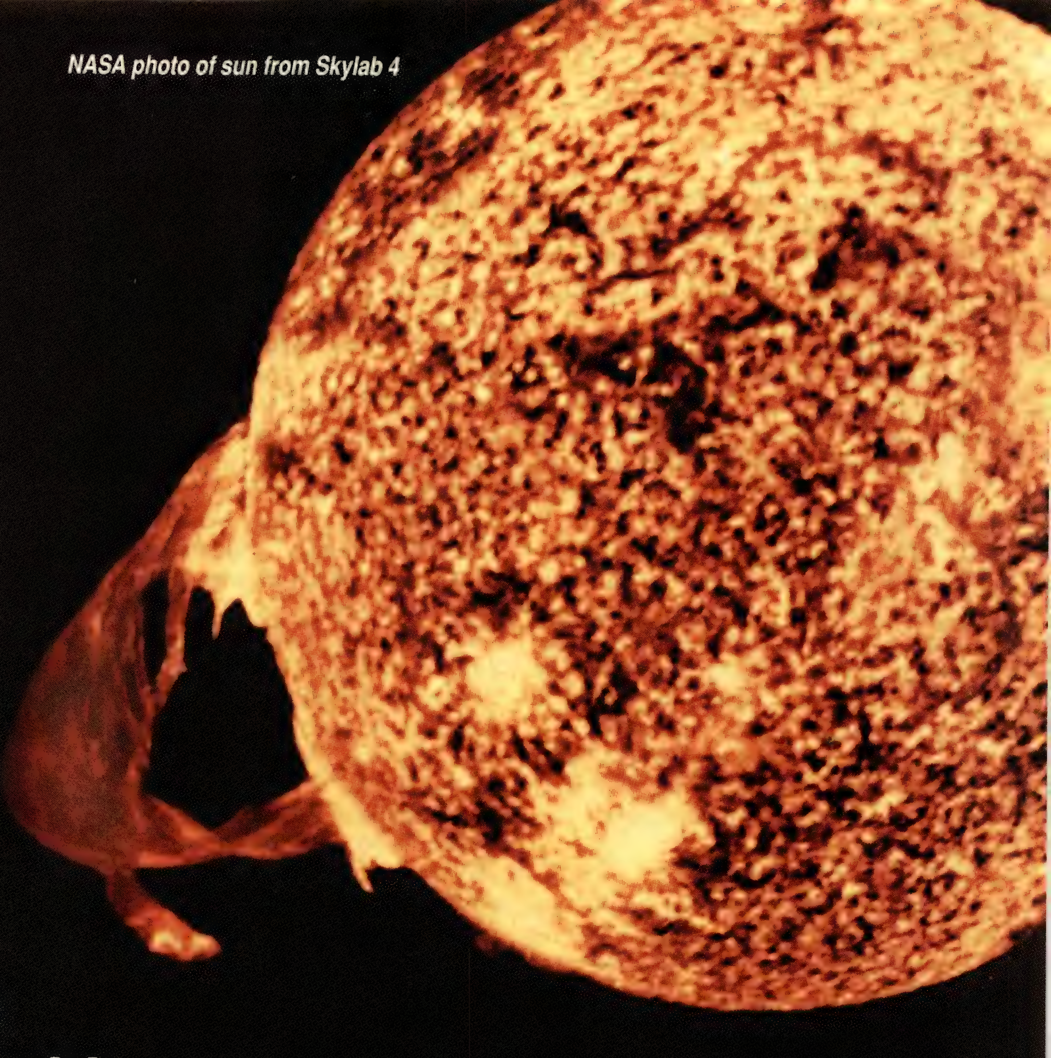
Spectra uses a synthesis tool to automate the creation of a BSP and a virtual target. If all of the device drivers for the new I/O devices are available, developers need only write a small specification file and execute the synthesis tool.

The synthesis process for building a virtual target for the Snakes Video game system, which has two virtual I/O ports that simulate serial inputs, is a good example *(Fig. 4)*. The virtual I/O ports, built with Unix sockets, are called KEYPAD_1 and KEYPAD_2. Each is connected to one keypad panel. Pressing a key on the keypad sends 1 byte to the virtual target.

A third I/O port, connected to the "virtual console," is standard on every virtual target, so it need not be specified when configuring a virtual target. A single re-entrant LDD is provided for both virtual ports.

The virtual I/O port consists of template and device driver files. The template file contains the data structure that describes the "on-board" socket-based I/O devices. The device driver file features three basic functions: creating and initializing the socket I/O device (*logio_device_init*); reading (*logio_device_read*); and writing (*logio_device_write*). The complete logio driver code contains only several hundred lines of code.

The *logio_device_init* function is called during creation and initial-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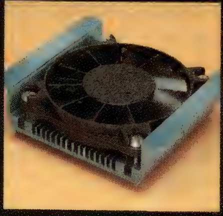

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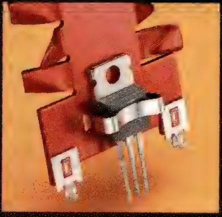

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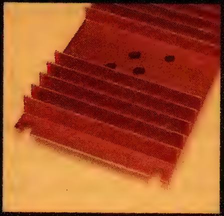

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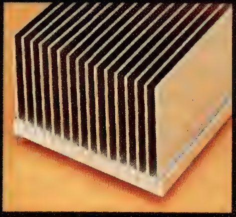

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ization of the device by the system. First, the Internet TCP/IP socket is created, and then the socket is assigned the port number supplied by the Unix system.

Next, during the device-specific initialization, the socket is made nonblocking, allowing for asynchronous I/O signals. After the *listen* command is executed on the socket, a flag is set showing that the socket is not yet connected.

The *logio_device_read* function reads from the virtual I/O port. If not connected, it executes the *accept* call to process any pending connections. If connected, it reads from the new socket and passes the buffer to the *logio_device_read* caller.

The *logio_device_write* function writes to the virtual I/O port. It writes the buffer to the socket.

SPEC FILE NEEDED

In this example, the specification file called *video_game.def* is required for the synthesis process *(see the listing)*. The first three lines of the specification are files with the rules for building the Sun4 (Sparc) virtual target using Sun's native compiler tools.

The rest of the file contains the values of the various properties, like the device type (for example, dev.keypad_1.type: socket), a list of the devices (board.devices.usr: keypad_1, keypad_2), a list of the files containing the device driver code (vtarget.objs.usr: ./socket.o), additional libraries, and the memory map specification. The synthesis tool uses this specification file along with device templates (such as ./socket.tmpl), and a knowledge base of general rules and templates (vtarget.def, vtsun4.def, devices.tmpl, and bootcnfg.tmpl) to generate the virtual target.

The time needed to configure and build the virtual-target prototype *(Fig. 4 again)* was about 24.5 hrs., including development of the device driver code. *(Table 1)*. If existing device drivers had been used, the time required would have been negligible. Even with device driver development, the time needed to build a virtual-target prototype can be two orders of magnitude shorter than the time needed to develop a traditional simulator.

The next step is to built a prototype of the virtual instruments for the video game system using the Spectra Virtual Instrument Prototyping system. In this process, Spectra relies on two portions of DataViews—DVdraw, an interactive drawing editor for creating customized user-interface screens; and DVtools, a runtime library of subroutines that manage and manipulate the display. Spectra uses DVdraw to quickly prototype the virtual instruments *(Fig. 5)*.

DVserver, which acts as Spectra's virtual instruments display executive, is a DVtools application that uses Spectra's logio interface to send and receive data over virtual I/O ports. DVserver is customized for an application by relinking it with a custom logio device driver. This driver is generated from the view file employing an included converter program that parses DataViews view files and builds a definition file to be used by the Spectra synthesis utility.

CREATING A VIEW FILE

A DataViews view file contains two essential parts: a list of graphical objects and a list of data objects. The first step in creating a view file to represent a virtual device is to specify the data objects. This step has two parts—creating a data source and specifying the record format for that data source. DVserver recognizes DataViews memory data sources named "portname.socket" to be logio data ports named "portname." The data type specifications must match those of the process that will write data to this port.

Graphical objects may have attached dynamics that are driven by data objects. When a view is "played back" in a DVtools display executive, such as DVserver, data objects are updated, and then graphical objects whose values have changed are redrawn. Details of how the data objects are updated and how graphical objects can be used to send data are built into the model of the display executive.

In DVdraw, object names can be 255 characters long. The DVserver display executive recognizes two special names. The first is "QUIT, Quit, quit: Terminate the DVserver program". The second is the send data command "S:portname:value_list," where portname must match a logio portname.socket specification and value_list is a comma-separated list of byte values and/or variable names.

For example, S:keypad:0,127 sends the byte values 0 and 127 over the logio port keypad.socket. And S:keypad:10,mode,0 sends the following values over the keyboard.socket port: byte 10, the mode variable, and byte 0.

A special converter program takes a DataViews view file as input and then outputs a Spectra specification file (for example, dvpad.def), which can be used by the Spectra synthesis tool. Next, the synthesis tool builds a "devices.c" file that's linked with dvserver.o to create a new executable, which is specific to the given view file. DVserver does employ the same logio device driver structure, and virtual instruments and the virtual target can use the same logio device driver code.

It took 25 hours to configure and build the video game's virtual-instruments prototype, including development of the DVserver code *(see Table 2)*. The time needed to configure the virtual instruments using existing device drivers and/or DVserver is negligible. Even with device driver development, it takes significantly less time to build a virtual-instruments prototype than to develop a traditional I/O simulator.

The complete debugging and testing process for the video game in the virtual development environment is shown in Figure 6. First, the kernel is built using the synthesis tool and loaded into the virtual target with a loading shell. After starting the kernel, the application program is compiled, loaded, and started.

At this point, a debugger is invoked from the loading shell. To examine the *get_inputs* task, a breakpoint is set and an input is generated by moving the cursor to the arrow button and clicking. Upon hitting a breakpoint, the *get_inputs* task is stopped to allow examination of the local variables.

Proper execution of the scheduler

is verified with a timing profiler. The profiler library is loaded to the virtual target and the monitoring process is initiated by running a monitoring shell. Captured samples are examined using the timing profiler. Any anomaly in the task's behavior shows up in a timeline task display.☐

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Nino Vidovic, chief scientist at Ready Systems Inc., received a PhD in computer science from the University of Zagreb in Croatia and an MS in computer engineering from Carnegie-Mellon University, Pittsburgh.

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CIRCLE

521 SIMPLIFY SYNC STRETCH CIRCUIT

BIAGIO PRESTI
Aptron Laboratories Inc., P.O. Box 323, Bloomington, IN 47402; (812) 336-4775.

During processing, a video sync signal will occasionally become compressed. This circuit, essentially made up of Q1, Q2, and Q3, comprises a video amplifier and sync stretch circuit *(see the figure)*. Q4 is an emitter follower that interfaces with following circuits.

Q1 sync strips the incoming video at a level determined by R_9. The incoming video is amplified and mixed with the stripped sync in Q2. Q3 provides inversion and video amplitude control via R_{15}.

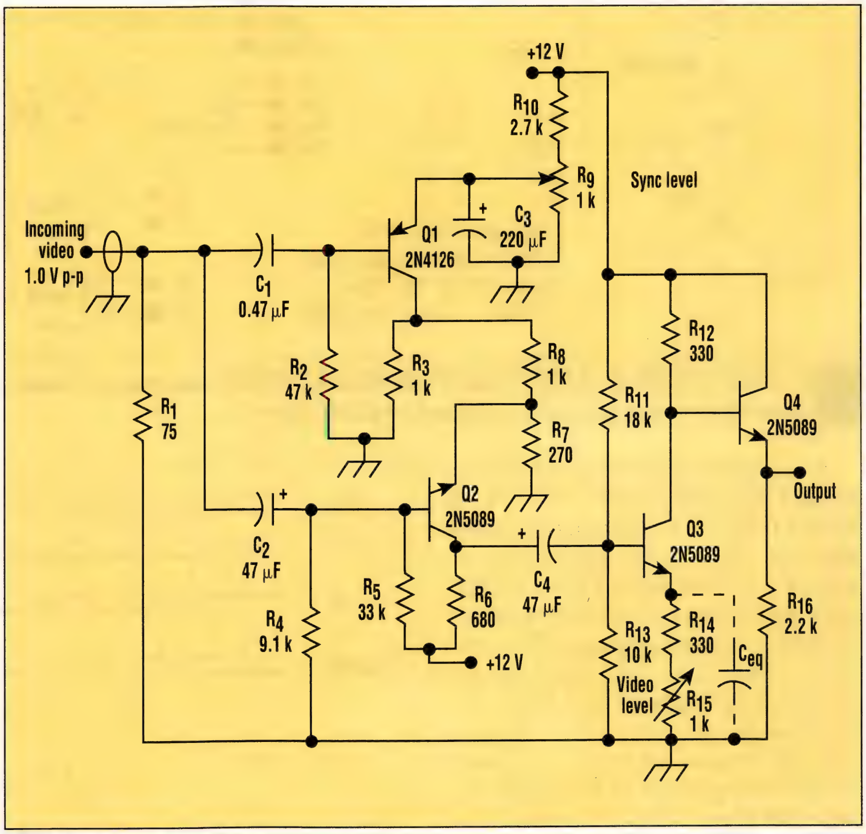
It may be appropriate in some circuits to provide a degree of high-frequency equalization through a small-value capacitor (C_{eq}), as shown in the figure, depending upon circuit layout.

In the setup, the sync level control (R_9) and the video level control (R_{15}) are used to set the ratio of sync to the video desired. They also set the output video at 1 V p-p.☐

IFD WINNER

IFD Winner for July 22, 1993

Craig B. Ziemer, AT&T Bell Laboratories, 2525 N. 12th St., Reading, PA 19612; (215) 939-6594. His idea: *"Build Solid-State Circuit Breaker."*



Q1, Q2, AND Q3 comprise a simple video amplifier and sync stretch circuit. Transistor Q1 sync strips the incoming video, which is amplified and mixed with the stripped sync in Q2. Q3 supplies inversion and video amplitude control.

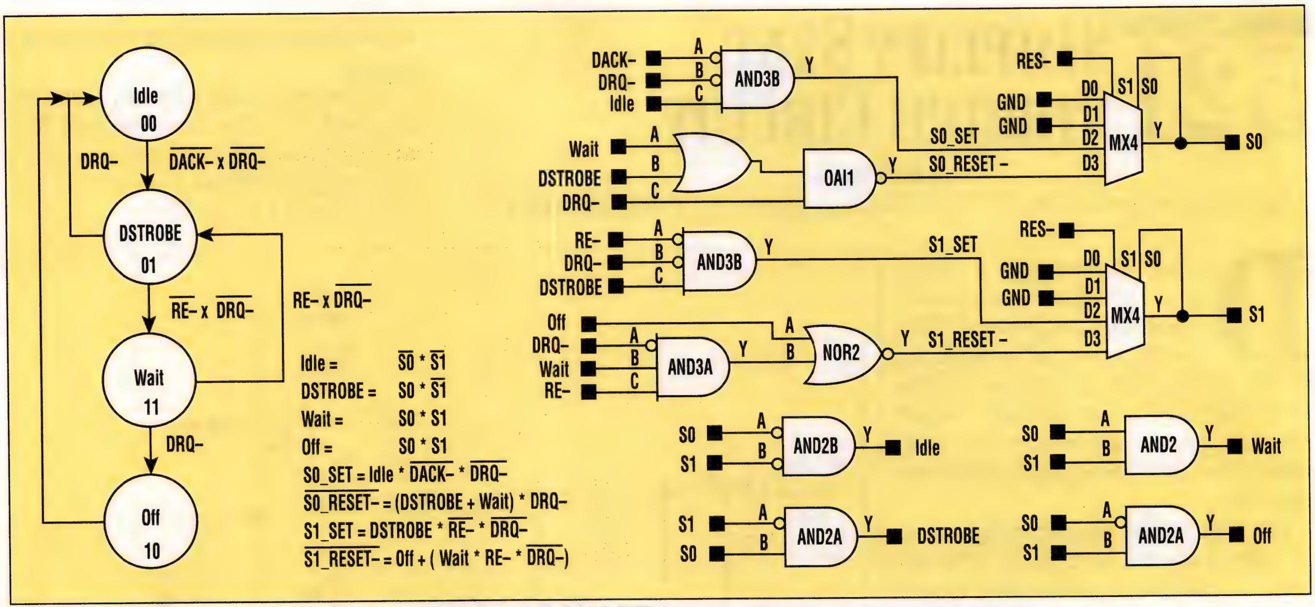
CIRCLE

522 ASYNCHRONOUS GRAY-CODE STATE MACHINE

GARY PEYROT
Pioneer-Standard Electronics, 5126 Clareton Drive, Suite 160, Agoura Hills, CA 91301; (818) 865-5808

State diagrams are a simple, yet elegant way to model complex systems, regardless of the implementation. Most state machines are designed to be synchronous. However, there are many applications that aren't well suited to a state machine that's limited to changing states on the edge of a clock. Such systems may require state transitions on both edges of a clock, or match dissimilar interfaces where state transitions must occur when control signals change levels.

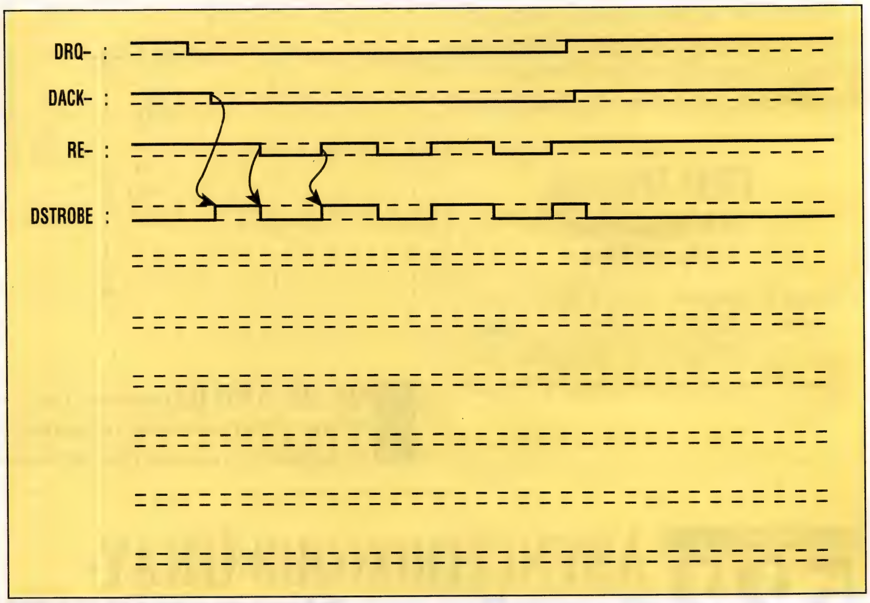
Asynchronous state machines have many advantages of their synchronous counterparts, but aren't limited to making transitions on a clock edge. One very simple state machine is the common SR latch. It has only two states, and transitions are made in direct response to the Set and Reset inputs without a clock. More complex systems require some precautions. With asynchronous transitions, care must be exercised to ensure that race conditions don't cause non-deterministic behavior. This can be done by encoding the states in a Gray code so that only a single state bit changes for each state transition. If more than one bit were to change, then skew would cause transitions through undesired states, causing glitches, oscillations, or unwanted state transitions. This precludes using a "one shot" implementation more common in FPGAs where each state corresponds to one storage element, because as one element turns off, the other turns on, and decoding glitches would result.


Idle
00
DRQ-
$\overline{DACK-}$ x $\overline{DRQ-}$
DSTROBE
01
$\overline{RE-}$ x $\overline{DRQ-}$
RE- x $\overline{DRQ-}$
Wait
11
DRQ-
Off
10
Idle = $\overline{S0}$ * $\overline{S1}$
DSTROBE = S0 * $\overline{S1}$
Wait = S0 * S1
Off = $\overline{S0}$ * S1
S0_SET = Idle * $\overline{DACK-}$ * $\overline{DRQ-}$
$\overline{S0\_RESET-}$ = (DSTROBE + Wait) * DRQ-
S1_SET = DSTROBE * $\overline{RE-}$ * $\overline{DRQ-}$
$\overline{S1\_RESET-}$ = Off + (Wait * RE- * $\overline{DRQ-}$)
DACK-
DRQ-
Idle
AND3B
Wait
DSTROBE
DRQ-
OAI1
RE-
DRQ-
DSTROBE
AND3B
Off
DRQ-
Wait
RE-
AND3A
NOR2
S0_SET
S0_RESET -
S1_SET
S1_RESET -
RES-
GND
GND
D0
D1
D2
D3
S1
S0
MX4
Y
S0
S1
AND2B
Idle
AND2A
DSTROBE
AND2
Wait
AND2A
Off

1. THIS SIMPLE, ASYNCHRONOUS GRAY-CODE state machine changes only a single state bit for each state transition to ensure that race conditions don't cause non-deterministic behavior.

An example of a simple, asynchronous Gray-code state machine is shown *(Fig. 1)*. As seen in the timing diagram *(Fig. 2)*, the application required a Strobe signal (DSTROBE) to be generated by transitions of two different control signals. The first strobe had to be triggered by the first falling edge of the DMA Acknowledge signal (DACK–). All subsequent strobes had to be triggered by the rising edge of the Read Enable Not signal (RE–). The state diagram models this behavior. The Off state is necessary because a transition directly from Wait to Idle would require two bits to change simultaneously. The S0 bit changes first in going to Off, then S1 changes going to Idle. The state storage elements are latches implemented as multiplexers. In a multiplexer rich architecture like an Actel FPGA, this circuit is very efficient.☐

Note: This work was done while Mr. Peyrot was a consultant with Three Step Development, West Hills, Calif.



2. A TIMING DIAGRAM illustrates that the asynchronous Gray-code state machine required a strobe signal (DSTROBE) to be generated by transitions of two different control signals. The first strobe is triggered by the first falling edge of the DACK- signal; all subsequent strobes are triggered by the rising edge of the RE- signal.

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CIRCLE 523

CURRENT AMPLIFIER BOOSTS OTA OUTPUT

ALEXANDRU CIUBOTARU
Univ. of Texas at Arlington, Dept of Electrical Engineering, Box 19016,
Arlington, TX 76019-0016.

A bidirectional precision current amplifier can be used to increase the output current of an operational transconductance amplifier, or OTA *(see the figure)*. The circuit is obtained from a simpler design[1] by adding a complementary stage and two

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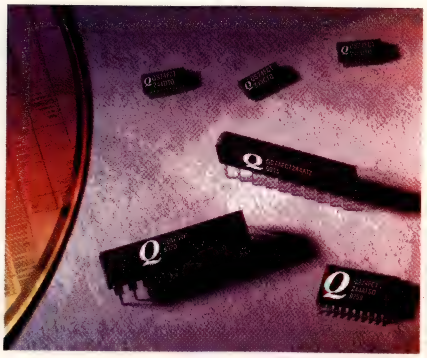

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diodes.

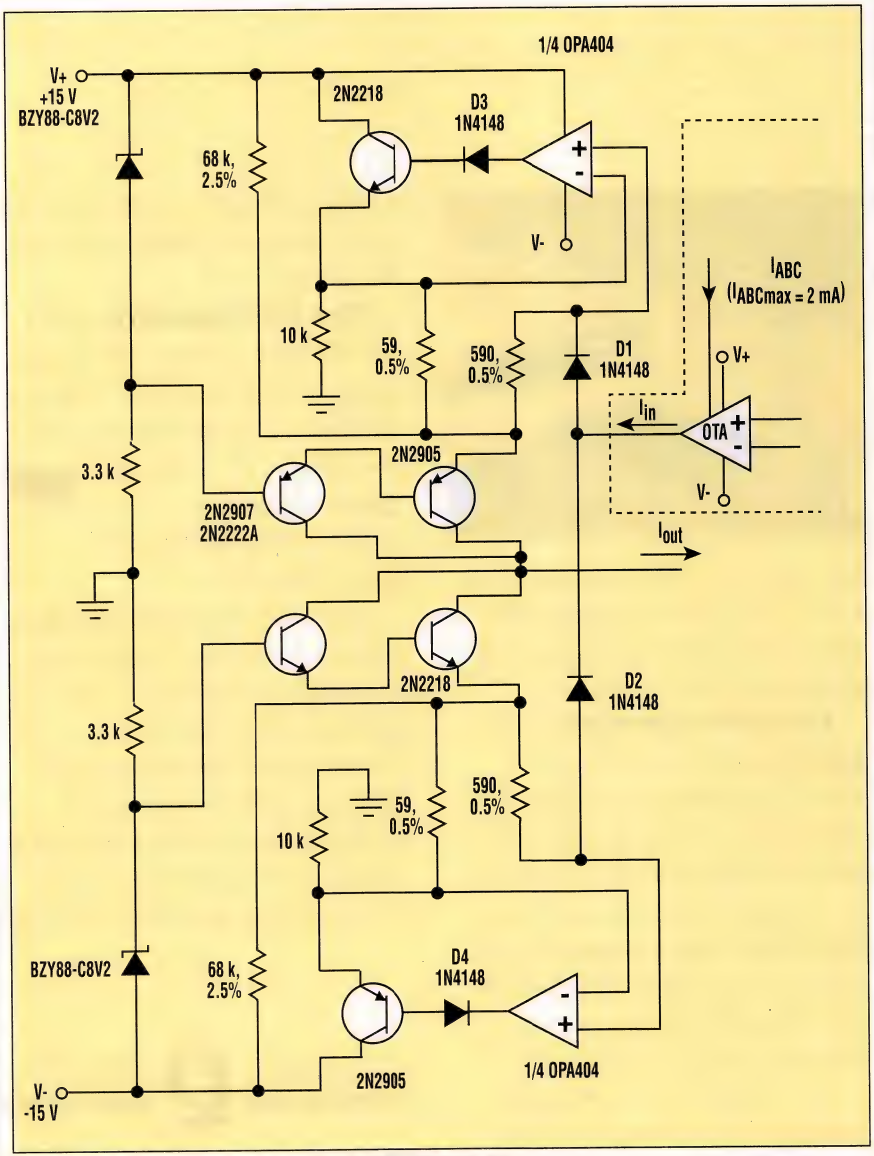
For positive input currents, diode D_1 is forward biased and the upper half of the circuit acts as a current amplifier for I_{in}. D_2, which is reverse biased and conducts no current, and the lower half of the circuit provide amplification for negative input currents.

The amplifier's current gain is 11 (set by the 0.5% tolerance resistors). Thus, the maximum output current has a value of 22 mA, if the maximum value is chosen for the OTA's I_{ABC}. Most OTAs require a bias current of less than 2 mA. The output offset current is less than 150 μA, with the output voltage range being –7 V to +7 V.

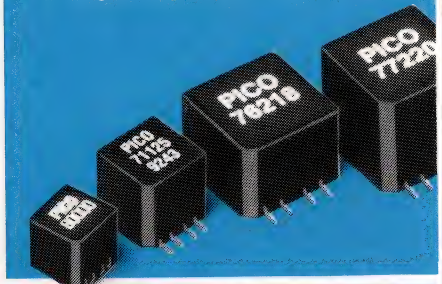
The circuit can be used with virtually no crossover distortion at frequencies up to several tens of kilohertz. Operation at higher frequencies is limited by the output capacitance of the OTA.☐

Reference:

1. Alexandru Ciubotaru, "D-to-A converter current booster," *Electronics World + Wireless World*, Sept. 1991; p. 755.



IMPLEMENTING A BIDIRECTIONAL precision current amplifier in an operational transconductance amplifier (OTA) can boost the OTA's output current. To accomplish this task, two diodes and a complementary stage are added to this otherwise simple design.



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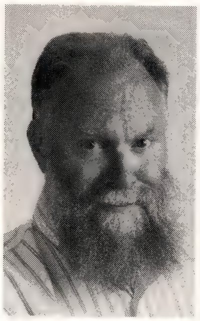
PEASE PORRIDGE

WHAT'S ALL THIS FUZZY LOGIC STUFF, ANYHOW (PART III)?

Let's jump right in and continue on with the Fuzzy Logic laundry list I started in the last issue.

20. F.L. is alleged to be "faster and easier to develop." That's what the F.L. guys like to claim. Again, I still don't really trust them. What would you expect them to say? Other engineers argue that the claimed ease and speed are not always there.

I am not in any position to prove this one way or the other, but you had best be on your toes, and insist on satisfactory comparisons. In other words, don't permit any straw men to be perpetuated. Or perpetrated.



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

Besides, even the proponents of F.L. admit that sometimes, tuning a F.L. system can take "hours or days of computer time...."[9] In a similar vein, Haubold vom Berg[10] cautions, "Be careful here, though: Applications for the possible use of fuzzy loops have to be carefully selected, and the degree of fuzzy control must be determined in advance. That's because a significant number of loops will not be optimized with a low-end fuzzy loop, and the instrumentation can be damaged."

Is it just possible that the optimization of F.L. controllers should not be left to the judgment of a technician with 15 minutes of training? Refer to the next paragraph....

21. F.L. guys claim that you do not have to be an expert to apply F.L. In fact, some of them say that any good technician can be taught in a few minutes to be an expert on Fuzzy-Logic controllers, replacing engineers with many months and years of schooling and experience.[11] Sure, they can say that any time, but I don't have to believe it. I am certainly not going to take this technician and set him in charge of my Nuclear Reactors. (Did they use Fuzzy Logic at Chernobyl?) (That's supposed to be a joke....)

22. F.L. guys claim that it is *easy* to put in the correct F.L. coefficients. If a ferry boat is heading for the dock, all you have to say is, "If velocity = (medium) and distance = (medium), then keep negative RPMs = (medium) to maintain the necessary deceleration."

Conversely, if an expert wants to set up a conventional control system, he has to know that the number of RPMs must be $K \times (1 + V - (2\,a\,x)^{1/2})$, where K = –860 rpm, with all parameters expressed in (feet) and (seconds). He has to be smart enough to know that K = –860, and not +860, or –86, –0.086, or –0.00086, or –460. But to make F.L. work, all you have to know is, to say "medium."

Well, don't look now, but if the conventional guy guesses wrong, at K = –86, and the ferry boat winds up perched on the dock, the F.L. guy can certainly make the same error, and HIS ferry boat will wind up on the dock, too. Hey, a factor of 10 error in either case will bring you to that same result. Fuzzy Logic computers are NOT clairvoyant. If you tell them to do the wrong thing, they will not just "do the right thing," they will do what you tell them. Magic is not an appropriate element to invoke, nor to depend on....

23. It is sometimes claimed that F.L. can "learn" how to get the right answer—this is supposed to be a big advantage. However, Fuzzy Logic by itself cannot "learn" anything. If you want to get the F.L. to "learn," you have to use adaptive F.L. (non-trivial) or use Neural Networks. The knowledgeable guys with NeuFuz4 showed me that if you use Neural Networks to find a solution, and set the Membership Function, and generate the rules, these rules may be non-heuristic, not at all the same old rules, but improved rules with new advantages. Sounds impressive. Call them for details.[12]

Still, if you want to run the F.L. in a learning mode, be aware that a F.L. controller may make a lot of mistakes as it learns. Again, this is not the place to let loose the F.L. controller on your brand-new Nuclear Reactor, or your new catalytic cracking plant, or your epoxy resin kilns. F.L. controllers can be coached to learn a task when you have saved up a lot of data on how the system runs. It can look at the input data and the output data, and figure out how to control the plant. *BUT* only if you have that data, for all relevant regimes of control.

If you have a nuclear reactor, and if you had a Fuzzy controller for all normal operating modes, you would NOT use F.L. to control the system in the case of a breakdown, emergency, blow-up, melt-down, loss of pressure, thermal run-away, or any other non-standard mode, because F.L. only works well when you have run your system in that mode, and have a lot of data on that mode. You don't want to engineer your control of emergencies that way.

24. Further, it is claimed that F.L. can adapt to changing systems—as if conventional controllers could not. But conventional controllers can operate with adaptive coefficients. You can take a conventional PID (Proportional-Integral-Derivative) controller, and add on adaptive or self-tuning

procedures. If you *know* the Control System Industry, you would know that. If you *didn't know* that, you might be willing to give F.L. some credit for miraculous advantages, which are not new advantages at all.

25. Remember the old saying, "To a man with a hammer, everything looks like a nail." Well, if a person knows how to apply Fuzzy Logic, and he doesn't know any other way to do it, I should not tell him that he cannot do the task. However, he has no right to tell me that is the only way, or the best way, just because it is the only way he knows....

26. F.L. has been stated[13] to be quite good at controlling the same kind of systems that people can, but with faster sampling, fewer mistakes, and more features. Anything you can do, slow as you are, a computer can do a little faster, better, and more consistently. Okay, that's not a silly statement: Anything I can do, that gets boring and repetitive, such as, starting and stopping a subway train smoothly and precisely, time after time, may be a good candidate for F.L. As far as I am concerned, that is arguably the best thing we can say about Fuzzy Logic.

27. Now, where are the cases where F.L. really is not suitable to do a good job? I suspect there are cases where the F.L. computing speed is not adequate, and maybe even a fast analog controller is necessary. Also, cases where timing, counting, integrating, and differentiating are required are not feasible unless you combine some F.L. and some conventional logic.

While we hate to be negative, it is important to be honest, because if there really are tasks that F.L. cannot do, we don't want to waste people's time on them. I think that F.L. people ought to make known, and *publicize*, cases where F.L. is really unsuitable, and, if possible, the reasons why. This is for the good of their industry.

28. Also, several people sent in reminders, that if you have a conventional controller, and it is working OK, there is usually not any advantage to throwing it out and replacing with a F.L. controller, despite all the HYPE to the contrary. Any case where F.L. is shown to provide a WONDERFUL advantage over a conventional control system, is either a case where the conventional controller was not at all optimized, or, the system was nonlinear so the conventional controller could not do well.

Lastly, let's look at a couple of specific examples about Fuzzy Logic.

29. By the way, nobody yet has recollected where the original magazine article was, that said that a Fuzzy Logic Controller could control a subway train smoothly, but a "conventional" digital controller would jerk, jerk, jerk, jerk... Does anybody recall seeing that—can you tell me where that was published? I did a search, but nothing turned up....

30. On American Public Radio,[14] Daniel McNeill stated that the new 1993 Saturn has an improved automatic transmission, so that on steep upgrades, it uses F.L. to cut out surging, "hunting," and excessive shifting up and down.

WELL, the Saturn's transmission *has* been improved, and it *does* use Fuzzy Logic to provide automatic downshifts on downhills. But the transmission does NOT use F.L. to avoid "hunting" on upgrades.[15] It uses conventional hysteresis. Fuzzy Logic is NOT needed to do that, and is NOT used for that.

31. Also, I have always been skeptical that F.L. can make a subway train run much more smoothly than a good conventional controller. In a recent magazine,[16] Bart Kosko admits that the conventional train control system that was compared to Hitachi's F.L. controller, in Sendai, Japan, was pretty crude and jerky. "Conventional controllers start or stop a train by reacting to position markers that show how far the vehicle is from a station... the automated controller will apply the same brake pressure when a train is, say, 100 meters from a station, even if the train is going uphill or downhill."

Well, if the best competing "conventional" control system was so shoddily engineered, and was not intelligent enough, not adaptive enough, to apply the brakes differently, if the train was going fast or slow, uphill or down, empty or fully loaded, then of course the Fuzzy Logic system deserved to win, but only by default, not by inherent superiority. If nobody had the sense to *move* the "apply brakes" markers 130 meters out, on a downhill, or 80 meters out, on an upgrade, then we are talking about relative levels of stupidity.

And Kosko observes, on the conventional controller, "because the controllers are rigidly programmed, the ride may be jerky..." Well, of course, a F.L. system can show advantages when compared to a system as crude as that, if nobody programmed the acceleration to feather off, to avoid $dv^2/dt^2 = da/dt$ = "jerk." Also, I heard statements that during quiet times when human operators drive the trains to keep in practice, riders can tell this because the acceleration is not as smooth.

Well, of course the planners reserved the smoothest modes for the Fuzzy Logic system, and left the operator-controlled system lurchy, so it could not be as smooth. What would you expect? So much for the Old Straw Man business.

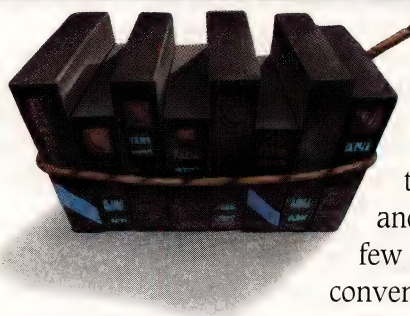
32. Also, some F.L. experts are *still* claiming that F.L. has some real inherent superiority over conventional (digital) controllers, because F.L. can represent a range of signals, whereas a conventional digital control system can only correspond to one ONE, or one ZERO.[17]

They still seem to be good at pretending that computers have only one bit—that computers do not have 8 (or more) bits in each digital word. Perhaps they try to perpetrate this story by pretending that Fuzzy Controllers work with miraculous awareness of the surrounding world, and do not depend on the *same* sensors and the *same* analog-to-digital converters that conventional digital controllers use.

If more people were aware that Fuzzy Controllers and Digital Controllers used the exact same input signals, the Fuzzy systems might seem less fantastic and revolutionary and amazing.

33. Even recently I heard of a system where F.L. engineers made a demonstration system to control the

WE HAVE A VERY SERIOUS IMAGE PROBLEM. TOO MANY OF YOU KNOW WHO WE ARE.



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height of a ping-pong ball above a stream of air. The F.L. system was claimed to have taken only 15 days to develop, vs. 30 days for the "conventional" PID controller, which gave inferior results.

So, it sounds as if F.L. excelled in a fair test... But, when you think about it, this is obviously a very nonlinear system. Of course it is not surprising that a linear conventional controller does poorly, trying to handle a nonlinear problem. Of course, a well-designed F.L. controller can do a better job accommodating this kind of nonlinear problem.

The Fuzzy-Logic controller was obviously showcased—set up to look good. But showing that a conventional controller could not do well despite "30 days of development effort," shows how much work these people were willing to put into setting up their Straw Man!!

34. So we still see plenty of places where F.L. promoters have engaged in HYPE, and we have probably not seen the last of it. But if we protest to the editors, and refuse to accept stonewalling, we can force editors to pay some attention to truth and honesty. For example, in the IEEE Control Society,[18] several people wrote in to the Editors, to protest about misleading claims about Fuzzy Logic. Maybe the Fuzzy Logic Industry needs an Anti-Hype Committee, to rap the knuckles of people who make preposterous claims?

35. Conversely, I have seen a few examples where F.L. is proposed to offer modest advantages, perhaps 1 or 2 dB.[19] Advantages like that are much more likely to be true and to be believed. I think it is great if F.L. can compete with the best existing systems and show advantages. If F.L. shows advantages when competing with obsolete systems, that should be admitted.

36. Several people pointed out that there are a lot of engineers and scientists working with Fuzzy Logic, and just a small fraction of them generate most of the hype. So I want to apologize to anybody who has been offended by my broad accusations: if *you* ain't guilty, then I wasn't talking about *you*.

37. At a recent Fuzzy Logic Convention, several people said, "I hope we don't see any more demonstrations with the Inverted Pendulum, because it's boring and not very relevant." Well, F.L. people are still bragging about their advantages in stabilizing the Inverted Pendulums—Single, Double, and Triple. Maybe if they don't want to hear any more about it, maybe that is exactly why I should do it, without Fuzzy Logic, as a counter-example?...

38. At that Fuzzy Logic Convention, it was suggested (by several people, not just RAP), that maybe a new name should be developed for F.L., to take away the stigma and the negative connotations.

Maybe there should be a contest for the best name for F.L. I'll chip in $10.00 for prizes, for the best new name. But in Japan, F.L. is not called by the name ai-mai, which means "fuzzy;" it is called, "Fa-Zhi." Maybe American promoters can figure out how to promote "ai-mai logic?"

39. In this vein, I talked to a smart engineer who has been earning his living, designing systems using F.L. His designs have been successful, and his clients have been delighted. So why can't he show me a good F.L. example? Because most of his recent clients have *forbidden* him to talk about his designs. Half of them were concerned that their competitors would find out how well the Fuzzy Logic worked—and the other half were scared that their customers would find out they were using Fuzzy Logic. Besides, he's too busy to show demos....

40. I do not think this is *the last word* on Fuzzy Logic, but I think we have at least raised the right questions. The answers will not come easily, because some of these people do not have much incentive to answer questions clearly.

But here's the situation as I see it. If we stick to our guns, then maybe we can instill enough honesty that people will be able to see where Fuzzy Logic really is appropriate.

Then, hopefully, they'll start to use it mainly for just those applications. And we really could use some concrete examples of where Fuzzy Logic is really good, and where it is *not* good. I'm still waiting, and so are the readers of this column. We'll be interested to hear your stories and letters.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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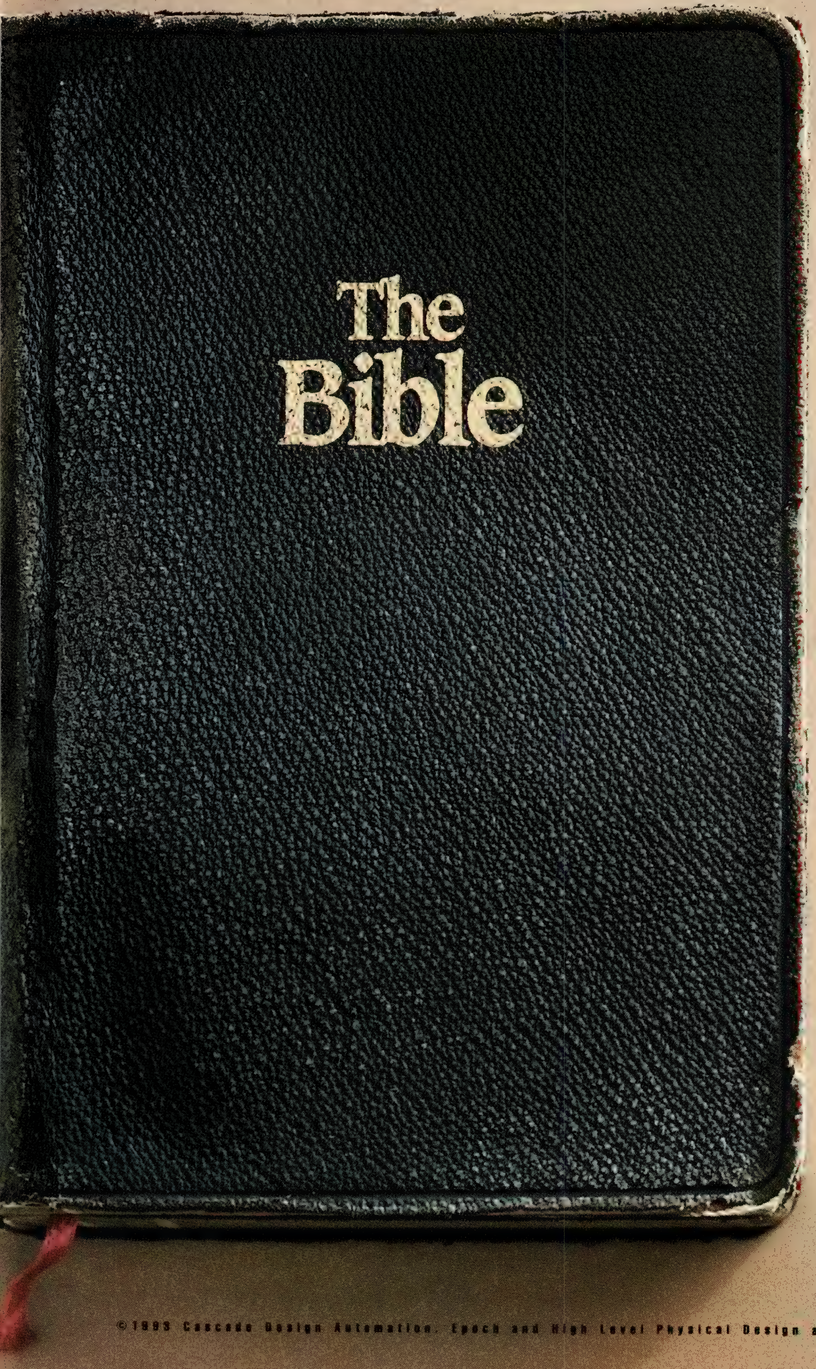

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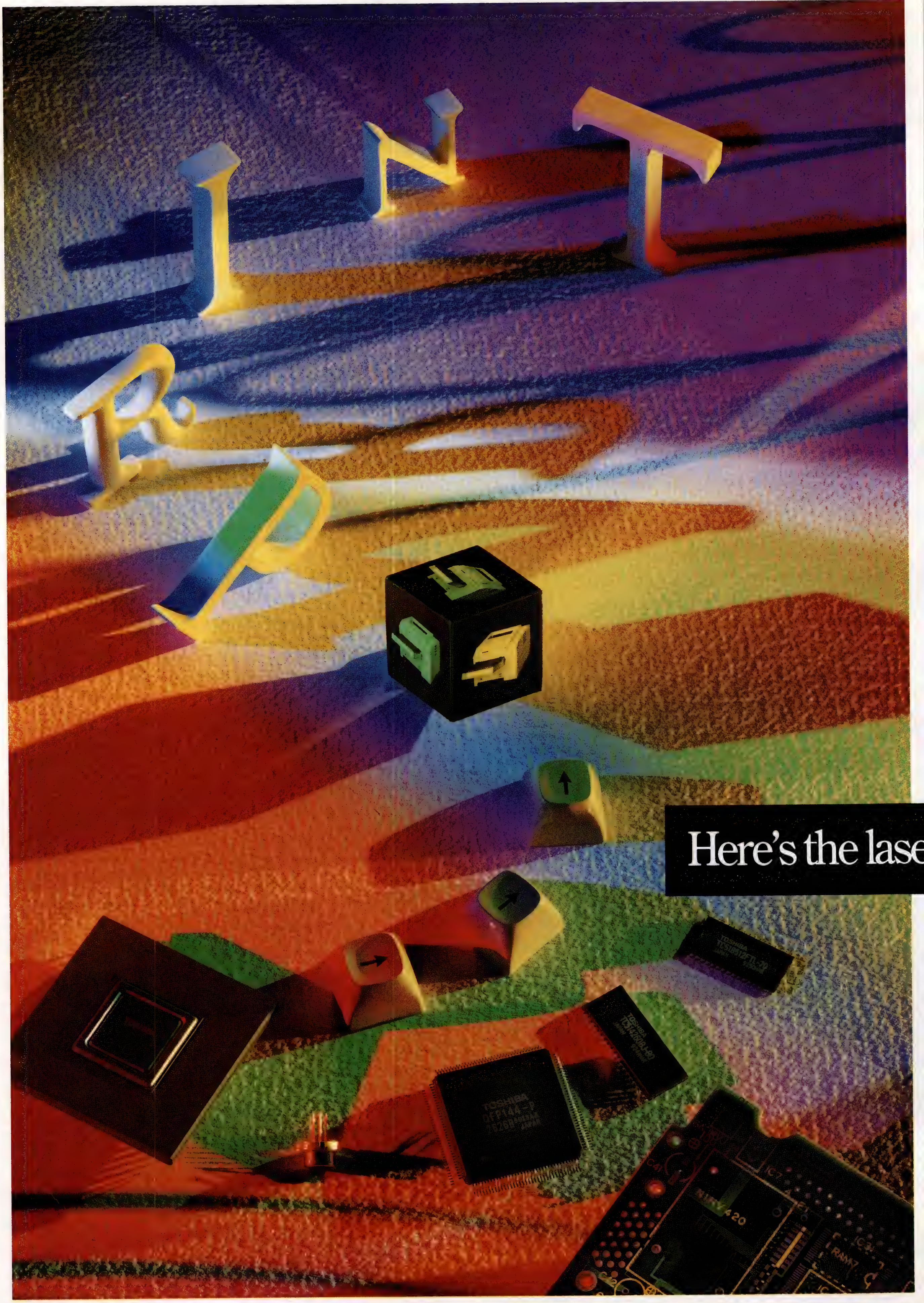
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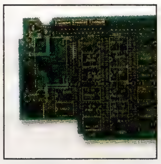
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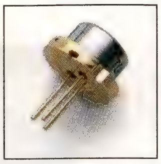
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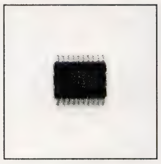
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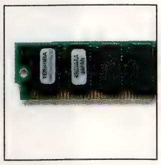
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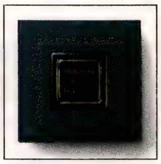
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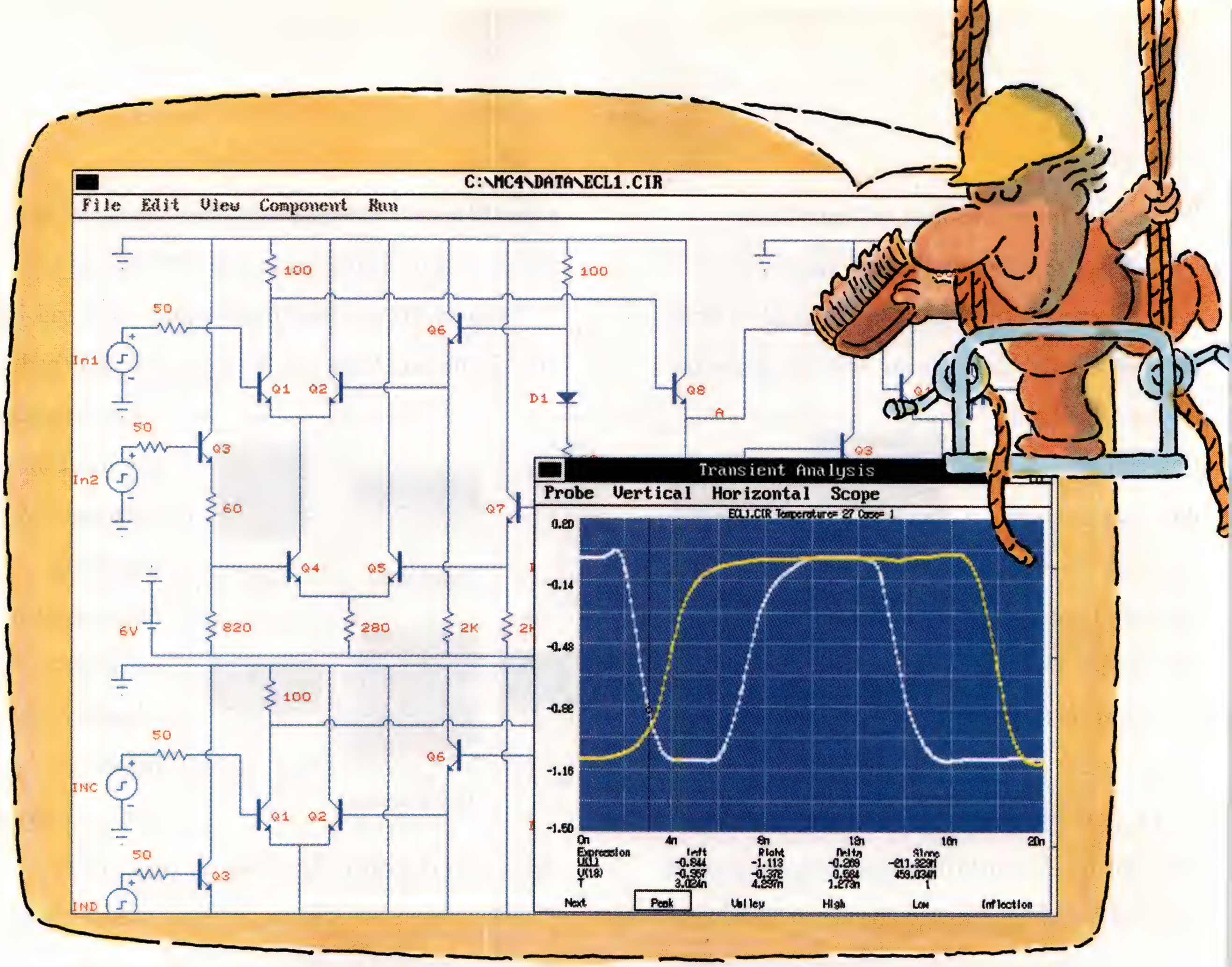

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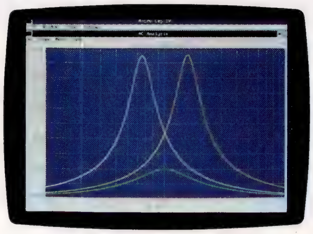
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EDITED BY SHERRIE VAN TYLE

MARKET FACTS

Sales of data-acquisition systems and software will more than double worldwide, increasing from $868 million last year to hit $1.8 billion in 1999, according to Frost & Sullivan Market Intelligence. The Mountain View, Calif., market researchers forecast that the plug-in boards will increase their market share from 79% of revenues to 82% by the end of the decade. Software will increase slightly, going from 8% to 9% of revenues.

PC-based data acquisition is making inroads in traditional data-logger and remote front-end markets. Plug-in boards are getting smaller, as are data-loggers, which are becoming more portable. As with most electronic equipment, boards are being developed that have increasing throughput and sampling speeds, as well as more intelligence in remote front-end units. Makers of plug-in boards are offering purchasers such incentives as free software drivers.

Competition will likely grow fiercer in this segment, say the researchers, with an industry shakeout probable in the general, rather than application-specific, market. The PC-based market is seeing new applications—agriculture, environmental monitoring, and atmospheric data-gathering—along with industrial process control. Constraining application development are problems with product flexibility and ease of configuration, the researchers say.

DATA ACQUISITION MARKET GATHERS STEAM AROUND THE WORLD

	Units in thousands	Revenues ($ million)
1992	609.9	868.1
1993	682.5	943.6
1994	768.8	1,035.0
1995	869.5	1,146.4
1996	990.3	1,281.1
1997	1,122.2	1,439.5
1998	1,260.0	1,612.2
1999	1,391.5	1,792.1

Compound annual growth rate (1992-1999) = 10.9%

Source: Frost & Sullivan Market Intelligence

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Packages	44 PLCC	68 PLCC	84 PLCC	100 PQFP	144 PQFP	160 PQFP	208 PQFP
	28 PLCC	44 PLCC	68 PLCC	84 PLCC	100 PQFP	144 PQFP	160 PQFP
PLCC	20 SOIC	28 PLCC	44 PLCC	68 PLCC	84 PLCC	100 PQFP	144 PQFP
PQFP	16 SOIC	20 SOIC	28 PLCC	44 PLCC	68 PLCC	84 PLCC	100 PQFP
SOIC					44 PLCC	68 PLCC	84 PLCC
						44 PLCC	68 PLCC

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BETTER WAYS FOR
GATE ARRAYS

How does Orbit slash per-unit cost on quantities as low as 100 pieces?

WHY PAY FOR AN
FPGA

QUICK NEWS: CONFERENCES & COURSES

A C Programming Hands-on Workshop, Advanced C Programming: Techniques and Data Structures, and C++ Hands-on Object-Oriented Programming are among the courses that will be held by the Learning Tree in various U. S. cities through the fall/winter.

For further information or to register, contact the Learning Group International, 1805 Library St., Reston, VA 22090-9919; (703) 709-9019; fax -6405; West Coast: (310) 417-8888; fax 410-1320. CIRCLE 460

The 1994 International Reliability and Maintainability Symposium will include workshops of joint application design, application of fuzzy logic, concurrent engineering, CAE tools, and test and evaluation. it will take place January 24-27, 1994 in the Anaheim (Calif.) Marriott Hotel. For information on exhibiting, contact Scien-Tech Associates, P. O. Box 3048, Sarasota, FL 34230-3048; (813) 355-5207; fax (813) 953-3175. To register, contact Joel Magnus, P. O. Box 765, Camden, NJ 08101; (609) 338-2442. CIRCLE 461

The course, Design for Manufacture of Hybrid Circuits for Microwave and High-Speed Applications, will be offered jointly by the University of Wisconsin and Rutgers University Jan. 12–14, 1994 and Feb. 16–18, 1994. The course concentrates on the practical design of hybrid microcircuits and multichip modules. Design principles in the manufacturing environment are emphasized. The January course is offered in Madison, Wis., and the February course in New Brunswick, N. J.

For further information or to register, contact Harold Green, Department of Engineering Professional Development, University of Wisconsin—Madison, 432 North Lake St., Madison, WI 53706 (800) 462-0876; fax (608) 263-3160. CIRCLE 462

Intermec Corp.'s independent users group will host a technical workshop on automated data collection at the Sheraton Harbor Island in San Diego Jan. 9–13, 1994. Attendees will participate in hands-on training in planning, installing, and managing hardwired and wireless bar code data communications. The four-day training event is $695. Contact Kimberly Lombard, Intermec Corp., 6001 36th Avenue W., P. O. Box 4280, Everett, Washington 98203-9280. CIRCLE 463

HOT PC PRODUCTS

Jeopardy Detector reveals data jeopardy periods created by the SmartDrive cache by monitoring DOS for situations where the File Allocation Table (FAT) and directory entries don't agree. If an application program crashes or the PC is rebooted, cross-linked files and data loss may occur if the PC continues to be used. A JPRDY.ZIP file has the Jeopardy Detection program and papers on cache writing techniques on Compuserve from LIB 14 of PCVENA. Users unable to download the file can order a disk from PC-Kwik for $6.50 shipping and handling by calling (503) 644-5644; fax (503) 646-8267. Contact PC-Kwik, 15100 SW Koll Parkway, Beaverton, OR 97006-6026. CIRCLE 464

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 443, 100 Prickly Pear Rd., Verdi, NV 89439; (408) 446-4458; fax (408) 253-6085

This column assembles information from three prior columns into a structure that graphically and algebraically links staffing to the cost of lateness.

In the last issue the relationship between delay in market entry, d, and the staffing ratio, S, was established. It is shown below:

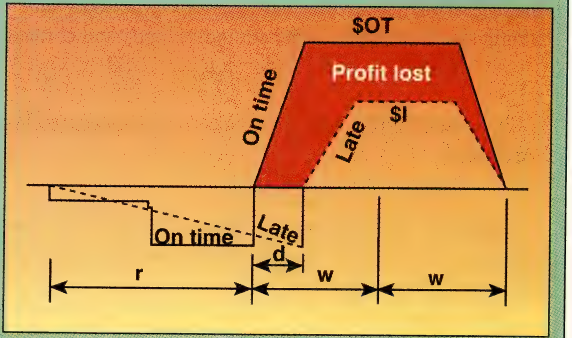
$$d = r(1 - S)/S$$

The staffing ratio ranges in value from 0 to 1. A value of 1 means that full staff is applied to get the product to market with no delay.

The August 5th issue supplied the insights on how the equation below was developed.

$$\text{Profit lost/profit on-time} - [w(3d + b - a) - d(d + b)]/[w(2w - a)]$$

This equation was derived for highly competitive business environments. Accordingly, "w" represents the market window; "d" the delay in entering the market; "a" the rise-time to and fall-time from mature on-time sales; and "b" the rise-time to and the fall-time from late entry mature sales. Substitution of values leads to the computation of the cost of lateness. The graphic link between the two equation was printed in the September 30th issue and is repeated here.



This collection of information makes it possible to compute the cost of delay as a function of new product development staffing through the use of the equations that are supplied. From a procedural perspective, determine the value of "S" and the value of "r" the on-time development time. Use these values to compute "d". With "d" known, substitute its value along with the values of "w", "a", and "b" into the second equation to compute lost profits, or the cost of delay.

I recommend working with a single numeric scenario to develop some skill in using the equations and the model. Once past this point, it is often times instructive to work with numerical values that span a range of possibilities. I encourage new product developers to enter this model into a hand-held computation device. As staffing and timing scenarios present themselves, you can use the model to help guide a highly leveraged new product development decision.

More information on this topic is contained in New Product Development: Design and Analysis, which can be obtained by calling Time to Market Associates.

QUICKLOOK

QUICK NEWS

Microsoft Windows NT Step by Step is a book-and-disk self-paced course on using Windows NT commands and features from Microsoft Press. In 30- to 45-minute lessons, readers learn to manage disks, directories and files in NT; share resources on a network; use Mail and Schedule+; and work with applications. Appendixes show how to install the operating system and protect data with built-in security measures. Developed with Catapult Inc., a Bellevue, Wash.-based, software training company, the courseware has an index and glossary. Windows NT is required; the course includes a 720-kbyte 3.5-in. disk. Contact Microsoft Inc., 1 Microsoft Way, Redmond, WA 98052-6399; (800) 677-7377 or (206) 882-8080. CIRCLE 465

TALES FROM A SKUNK WORKS

The question this time around is: why does all this matter? Skunk works, creating products, and changing the world—or industry at least—is hard work. Why should we bother? And is it worth the effort? The answer starts in a white paper by a MITI working group titled "Japan's Vision for the decade: 1990s." Japan seeks high value jobs for its workers. After exhaustive thought, the group postulated four criteria to target key industries: 1) high value added, 2) high growth, 3) high elasticity of demand, and 4) industries with high complementary leverage.

Seven industries meet these criteria. All are knowledge-based. All include a major manufacturing component: *microelectronics, biotechnology, general aviation, materials science, telecommunications, machine tools and robots,* and, finally, *computers and software.* Cold war has shifted to economic war, and these key industries will be the battleground.

The Japanese believe that those who control these industries will control world wealth and power in the 90s. The Germans went through a similar planning exercise. Guess what? They came up with similar criteria and the *same* list.

> "While the war metaphor may be troubling, it is not inapt. The war jeopardizes our standard of living, jobs, livelihoods, and self-esteem both individually and nationally."
>
> Marv Patterson, Hewlett Packard, 1993

> "It is much harder to nullify the results of an economic conquest than those of a military conquest."
>
> Korekiyo Takahashi, 1936

Global business is no longer a game. The success that you and your employers have in the marketplace will decide things more sacred than quarterly earnings or paychecks. It's war and our side is losing.

Unfortunately, as a nation we mostly don't know we are at war. We are not well equipped to fight if we did. Our national policy says that it doesn't matter if we build things or what we build. Our media reports simplistic events, not complex structural decline. Our government is inept at trade matters, and many officials take payment from foreign lobbyists. Our companies are mostly obsolete and whole industries are gone or hollowed out.

Did you ever consider how futile it is to balance trade by treaty, when the real problem is that we don't build products? At best this results in foreign-owned assembly plants and more exports of raw materials, not in family wage jobs.

These things will change. Our core asset is a base of trained developers of innovative technology-based products, and that is still intact. It's you, dear readers. Skunk works will be weapons shops for winning this trade war, and you will work there. I wish you the best.

John D. Trudel lectures and provides business development consulting. Trudel is founder and director of The Trudel Group, 52001 Columbia River Hwy., Scappoose, OR 97056; (503) 690-3300; fax (503) 543-6361; e-mail address: JohnTrudel@aol.com. He is the author of High Tech with Low Risk. *To order, phone (503) 280-8547.*

BEST SELLERS

What are the best-selling electronics and computer science books in Silicon Valley?

ELECTRONICS

1. *Art of Electronics*, 2nd ed. by Paul Horowitz and Winfield Hill. Cambridge University Press, 1990. $59.95.
2. *Art of Electronics Student Manual* by Paul Horowitz. Cambridge University Press, 1992. $27.95.
3. *Basic Electronics*, 7th ed. by Bernard Grob. Glencoe, 1992. $47.95.
4. *JPEG Still Image Data Compression* by William Pennebaker. Van Nostrand Rinehold, 1992. $59.95.
5. *Antenna Engineering Handbook*, 3rd ed., by Richard Johnson. McGraw-Hill, 1993. $119.50.

COMPUTER SCIENCE

1. *TCP/IP Network Administration* by Craig Hunt. O'Reilly & Associates, 1992. $29.95.
2. *Object Oriented Technology: A Manager's Guide* by David Taylor. Addison-Wesley, 1991. $20.50.
3. *Object Oriented Design with Applications* by Grady Booch. Addison-Wesley, 1992. $48.50.
4. *Testing Computer Software*, 2nd ed., by Cem Kaner. Van Nostrand Reinhold, 1993. $29.95.
5. *Code Complete* by Steve McConnel. Microsoft Press, 1992. $35.

This list is compiled for *Electronic Design* by Stacey's Bookstore, 219 University Ave., Palo Alto, CA 94301; (415) 326-0681; fax -0693.

EYE ON ISO 9000

The Malaysia manufacturing facility of Fujitsu Microelectronics Inc.'s Electronic Components Div. has been certified to ISO 9002 for the manufacture of electromagnetic relays, connectors, and computer keyboards. The company has its headquarters at 3545 North First St., San Jose, CA 95134; (800) 642-7616 or (408) 922-9000; fax 428-0640. CIRCLE 466

Amoco's high performance polymer production facilities have been certified to ISO 9002. The certification is for the company's Marietta, Ohio plant, which manufactures sulfone-based polymers. The company has its headquarters at 4500 McGinnis Ferry Rd., Alpharetta, GA 30202. CIRCLE 467

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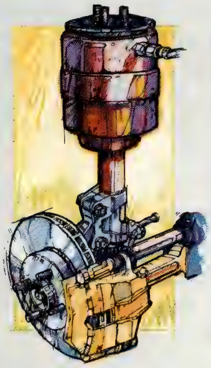
For over thirty years Allegro has been an IC supplier of choice for automotive manufacturers and sub-system suppliers worldwide. Allegro seeks to create value-added solutions for its automotive customers via merged-technologies. Extensive R&D resources are dedicated to the development and enhancement of automotive-specific processes enabling our engineers to incorporate Hall-effect sensing, logic, and power onto a single chip, in any combination, to meet each customer's unique system requirements. The results are ICs that achieve the highest levels of integration and are well matched to the rigorous quality and reliability demands of automotive applications.



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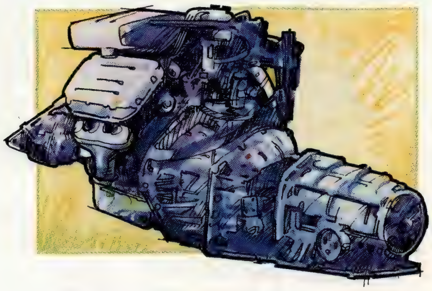
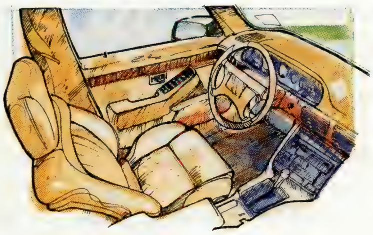
- Hall-effect Wheel Speed Sensors
- Hall-effect Height Position/ Steering Direction Sensors
- Fully-Protected Power IC Lamp and Inductive Load Drivers
- Mixed Signal ASICs for Signal Conditioning



INSTRUMENTATION

- Fully-Protected Power IC Lamp & Inductive Load Drivers
- AM/FM Stereo Decoders & Noise Blanker Signal Processing ICs
- H-Bridge Power ICs for HVAC & Gauge Control
- Hall-effect Window Position Sensors
- VF/LED Display Drivers



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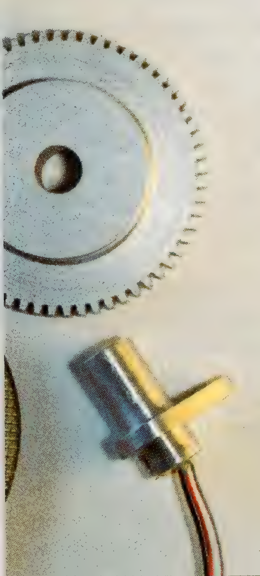


PC GRAPHICS WATCH

LOOKING BEYOND THE VAFC

MICHAEL ESKIN, BROOKTREE CORP. AND HOSSEIN YASSAIE, VIDEOLOGIC

The Video Electronics Standards Association (VESA) unveiled two new specifications for the low-cost integration of video into PCs: the VESA Advanced Feature Connector (VAFC) and the VESA Media Channel (VM-Channel). Historically, this integration has been accomplished on graphics cards using the 8-bit VGA feature connector. Unfortunately, this connector is limited to delivering video data at an 8-bit pixel depth on a display with a resolution of 640 by 480 pixels.

The VAFC breaks through the 640-by-480 barrier by supplying a dual-clocked 150-Mbyte/s, 32-bit bidirectional data path that enables video overlay on displays of up to 1024 by 768 pixels at 24-bit/pixel depths. Dedicated FIFO control lines allow asynchronous delivery of video pixel data to graphics data. Genlocking to an external video source is accomplished using a dedicated clock input pin.

The VAFC allows a video device to connect directly to the new crop of dual-ported RAMDACs on the graphics board and to easily support overlay features, such as those found in Microsoft's Video for Windows. This specification enables both PC-motherboard and graphics-card OEMs to integrate near-broadcast-quality video overlay and print-to-videotape into their high-resolution graphics systems for minimal cost.

The VM-Channel was developed to fulfill the future needs of multimedia on both PCs and workstations. VM-Channel is a dedicated multidrop highway connecting video, audio, and graphics I/O subsystems in a high-bandwidth, low-latency environment to transport compressed and uncompressed real-time data streams. The VM-Channel allows video data to be "broadcast" within a platform.

The cost effectiveness and transparent integration of video and graphics result from the single frame-buffer approach in the VM-Channel. The VM-Channel decouples the respective graphics and video rates and allows video data to be fed directly into a conventional graphics frame buffer. This means that video streams can be transported at their native rate, regardless of the host system's resolution or refresh rate. This method of attaching video devices eliminates the need for frame buffers in those devices.

While the VM-Channel is based on a single frame-buffer architecture, it intentionally avoids direct employment of the graphics-memory interface basically for two reasons. First, the graphics memory subsystem is highly configurable. Therefore, specifying a memory interface would hinder future developments.

The second reason is to maintain scalability of the interface in terms of channel width and complexity. The ability to target different cost/performance points is important to the graphics controller (which usually serves as the VM-Channel bus controller) as well as low-end video digitizers and codecs.

Within a VM-Channel environment, real-time data is transported as streams, which carry an ID header. The stream's ID is used by a source or destination to help direct the stream, such as pixel format and scaling attributes, to its correct path. This approach avoids the need to transfer large amounts of related attribute data with each stream, and offers a flexible and open method of handling or extending the system's capabilities. In particular, other real-time streams, such as audio, can be transported within the VM-Channel framework.

Moreover, with the VM-Channel, multiple devices can be combined in a modular fashion, an important feature both in terms of maintaining flexibility and reducing cost. For example, a base platform with a graphics subsystem that supports the VM-Channel can easily and cost-effectively be configured as a capture, decode-only, encode-only, or a full encode-decode video system. Furthermore, a VM-Channel-based system can handle multiple video-stream transactions between video subsystems, or between a video and a graphics subsystem. This becomes important in applications that support multiple video windows, such as video-teleconferencing.

The scheduling of stream-transaction activities on the VM-Channel guarantees access for each agent on the channel for a specific time period. Also, the handover mechanism, which passes the channel from one device to another, offers flexibility in selecting the next device. This "constrained" token-passing scheduling scheme supplies a simple, yet powerful channel-sharing mechanism that doesn't require any dedicated arbitration signals.

Both the VAFC and the VM-Channel are completely independent of the host bus, which means they can be employed in conjunction with any system bus, including ISA, EISA, VL-Bus, PCI, NuBus, and so on. For more information about the VAFC, the VM-Channel, or any other graphics-related topic, contact the VESA office at (408) 435-0333.

SYSTEM DESIGN NEWS

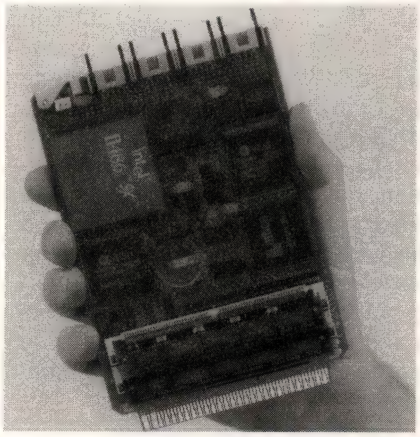
Leveraging off the previous release of a two-chip motherboard logic chip set for AT-bus 486-class personal computers, the Strauss chip set designed by Symphony Laboratories, Santa Clara, Calif., adds a third chip to provide PCI-bus compatibility. The trio of chips consists of the SL82C491 main memory and cache controller, the SL82C492 ISA bus and peripheral controller, and the SL82C495 peripheral-component-interconnect bus-bridge circuit. The first two chips, which form the previously released Wagner chip set, perform all of the functions needed to support four banks of DRAM (256 Mbytes, maximum); up to 1 Mbyte of write-through or write-back cache; support for 128 kbytes of system-management-mode memory; power-management logic for "green" PC and notebook capabilities; and integrated on-chip DMA controllers, interrupt controllers, and timers. The PCI bridge chip supports four PCI bus masters and includes a four-level FIFO buffer with PCI bus arbitration and error-handling logic. To implement a combination PCI- and AT-bus motherboard requires the three 160-lead chips in the Strauss chip set and just seven simple TTL chips to glue them together. The Strauss chip set sells for $22/set in lots of 10,000 sets. Contact Jack Yuan at (408) 986-1701.

A family of burst SRAMs that can keep sequential accesses to just 9 ns offers versions that support Pentium, 68040, PowerPC, and i486 cache subsystems. Developed by Paradigm Technology Inc., San Jose, Calif., the PDM44259S and L and the companion PDM44659S and L are organized at 32 kwords by 9 bits and come in versions that operate at system clock rates of 66.6, 60, 50, 40, and 33.3 MHz. Clock to data-valid times start at 9 ns for the fastest option, but versions can also be had with times of 10, 12, 14, or 19 ns. The burst memories come in 44-lead PLCCs and in either 5- or 3.3-V power-supply options. The SRAMs possess a self-timed write cycle and pack an internal burst-read/write address counter. Optimized for the Intel and Intel-compatible processors, the 5-V version of the PDM44259 gives designers a choice of standard operating current levels of 240 mA (9 ns version) or a lower-current version that trims about 10 mA (S and L suffixes, respectively). On standby, the SRAMs draw 90 mA for the standard version and 80 mA for the lower-current version. The PDM44659S and L, which handle 68040-style interfaces, have identical operating and standby current levels. Samples of all four chips are available. The highest-speed, 9-ns, 5-V version sells for $47.50 each in lots of 100. Call Zwie Amitai at (408) 954-0500.

By monitoring a CPU's temperature and its operations in real time, designers at Elitegroup Computer Systems Inc., Fremont, Calif., created a power-control scheme that can reduce system power consumption to less than the 30 W, thus meeting the EPA-established Energy Star power levels. Dubbed PowerShift, the scheme can enhance CPU performance by 20% or more, yet it trims power and keeps CPU temperature to 70°C for 486-class systems and 85°C for Pentium systems. The closed-loop system employed by the PowerShift scheme uses a customized version of the 8051 microcontroller to monitor the motherboard, disk drives, and power supply. When these components are inactive, PowerShift slows them down without putting them into a "sleep" state. By not putting them into a sleep state, the system can respond faster to outside conditions, which eliminates delays or no-response situations. The PowerShift scheme can also shut down inactive monitors and printers if those devices are designed to respond to the PowerShift software commands or the appropriate signals are incorporated into the motherboards. Elitegroup will incorporate the PowerShift technology into ISA, EISA, MCA, VL-bus and PCI-bus motherboards that use 486 and Pentium processors. This will be done by adding a small connector into which a PowerShift control module can be inserted. Furthermore, Elitegroup will offer licenses for the PowerShift scheme to other companies. Contact Darwin Chang at (510) 226-7333.

▼ STD 32 SBC HANDLES LOW TEMPERATURES

Low temperatures are no problem for the ZT 89LT02 STD 32 single-board computer (SBC): It's operating temperature range is from –40 to +70°C. The board combines various 486-processor choices with a local-bus video option. Built to a compact 4.5-by-6.5-in. form factor, the board's 32-bit local bus supports Super VGA and flat-panel displays, operating at CPU speeds. The board can run DOS, Windows, Unix, OS/2, QNX, and other operating systems. It can hold up to 8 Mbytes of DRAM and 2 Mbytes of flash memory, as well as a parallel and two serial ports. Available now, the ZT 89LT02 starts at $1975 (in 25-piece quantities) with a 25-MHz 486SX CPU and 4 Mbytes of DRAM.



Ziatech Corp.
3433 Roberto Ct.
San Luis Obispo, CA 93401
(805) 541-0488
▶CIRCLE 814

▼ VL-BUS GRAPHICS BOARD BOASTS LOW PRICE TAG

Offering a performance level of 23 million Winmarks, the VideoSpectrum VL is a low-cost graphics accelerator that plugs into the VL-Bus local bus. The $199 board is built with a Cirrus Logic 5428 accelerator chip that supplies 24-bit color output featuring 16.7 million colors. It comes with 1 Mbyte of memory and drivers for Windows 3.1, AutoCAD, Lotus 1-2-3, Microsoft Word, WordPerfect, and Wordstar. The VideoSpectrum VL is available now.

Cardinal Technologies Inc.
1827 Freedom Rd.
Lancaster, CA 17601
(717) 293-3000
▶CIRCLE 815

▼ BIOS REDUCES POWER DRAW OF SYSTEMS

Low power is becoming an important feature in desktop computers as well as portable systems. The Megakey Green PC keyboard BIOS contributes to the low-power movement by complying with the Energy Star specifications for low-power systems (the Energy Star program, run by the EPA, states that the monitor and platform each must consume less than 30 W in a sleep mode). The BIOS supplies operating-system and chip-set-independent power management. It controls the display, printer, video synchronization signals, and the CPU clock by setting independent standby timers in the BIOS setup. Megakey, available now, operates with standard, off-the-shelf chip sets to keep design costs to a minimum.

American Megatrends Inc.
6145-F Northbelt Pkwy.
Norcross, GA 30071
(404) 263-8181
▶ **CIRCLE 894**

▼ SCSI HOST ADAPTER HAS NO SWITCHES

Bundled with automatic configuration software and a switchless design, the ISApport SCSI host-adapter board is free of jumpers or DIP switches. The board is compatible with most SCSI-based peripherals, including CD-ROM drives, hard-disk drives, optical drives, and tape drives. The board is built with a floppy-disk controller to handle almost any type of floppy drive. It also features a 128-byte FIFO that buffers read and write data between the host system and the SCSI device. Data transfers take place at 5 Mbytes/s. The ISApport supports ASPI (Advanced SCSI Programming Interface) and CAM SCSI software standards and comes with drivers for MS-DOS, Windows 3.1, OS/2, Netware, and SCO Unix. It sells for $199.

Acculogic Inc.
13715 Alton Pkwy.
Irvine, CA 92718
(714) 454-8527
▶ **CIRCLE 895**

▼ ACTIVE-MATRIX LCD SPORTS 24-BIT COLORS

Designed for multimedia applications, the LC-10V1 is a 10.4-in. active-matrix color LCD panel. It supports full 24-bit color for more than 16 million hues. In addition to displaying computer-generated text and graphics, the LCD can display video from various sources, including televisions, VCRs, and laser-disk players. This makes the panel suitable for video-teleconferencing and security and presentation systems.

A built-in microprocessor can automatically adjust the panel for off-center images. In RGB mode, variations in analog output levels are handled either automatically, or manually by the user. The LC-10V1 is available now; connecting cables for most popular systems are sold separately.

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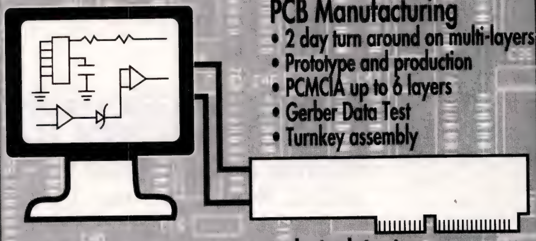

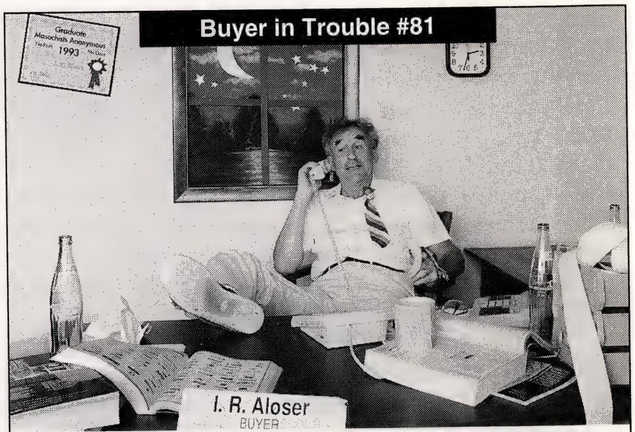

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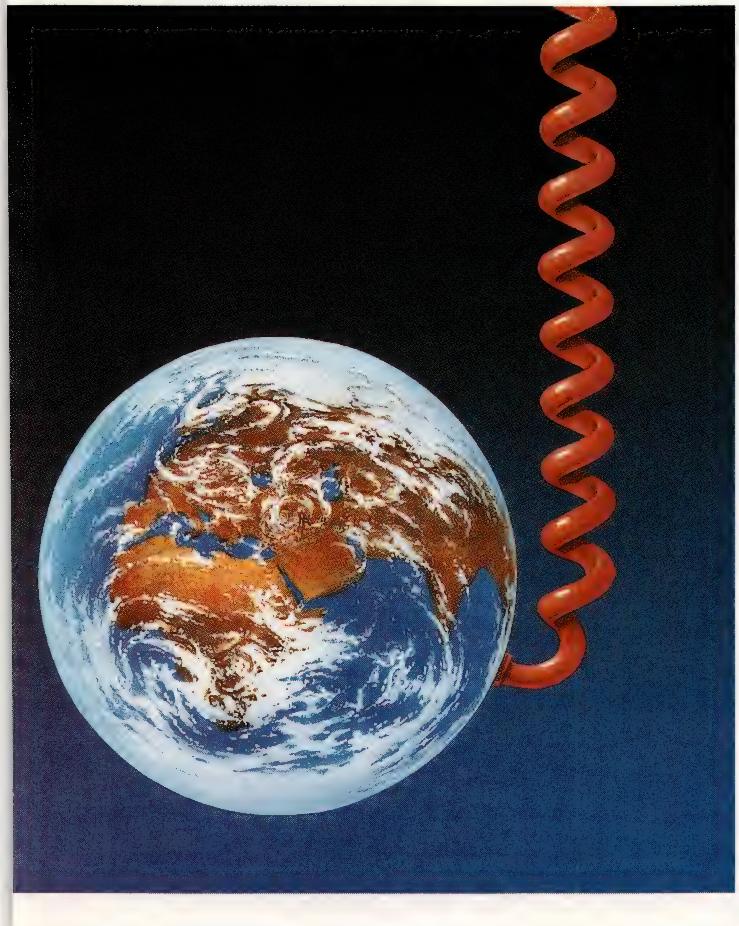

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▼ VAFC-COMPATIBLE RAMDAC RUNS AT 135 MHz

Video-ready functions and VESA Advanced Feature Connections (VAFC) compatibility both appear on the CL-PX2085 MediaDAC 24-bit RAMDAC. The 135-MHz chip supports four independent full-motion video windows. It also facilitates the full digital mixing of high-resolution graphics and full-motion video. In addition, it's compatible with most data-compression schemes.

The chip's YUV-to-RGB color-space converter delivers 24-bit full-motion video, while lookup tables allow brightness and contrast control. As a result, users receive full-motion video windowing and 1280-by-1024-pixel color resolution. Other advanced features include tag processing, individually zoomable windows, interpolated zooming, and single pixel resizing precision.

The CL-PX2085 is register-compatible with the popular BT485 RAMDAC and will interface with all VAFC video cards. The chip is housed in a 160-pin quad flat pack. It's sampling now, with volume production planned for early 1994. In quantities of 1000, the 24-bit RAMDAC sells for $50 each.

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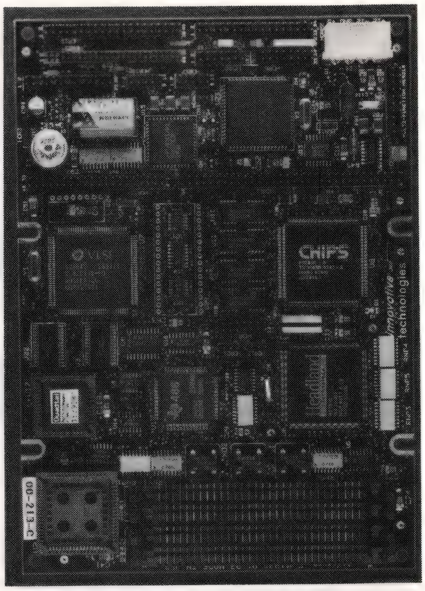
Innovative Technologies Inc.
P.O. Box 90086
Houston, TX 77290
(713) 583-1141
▶CIRCLE 898



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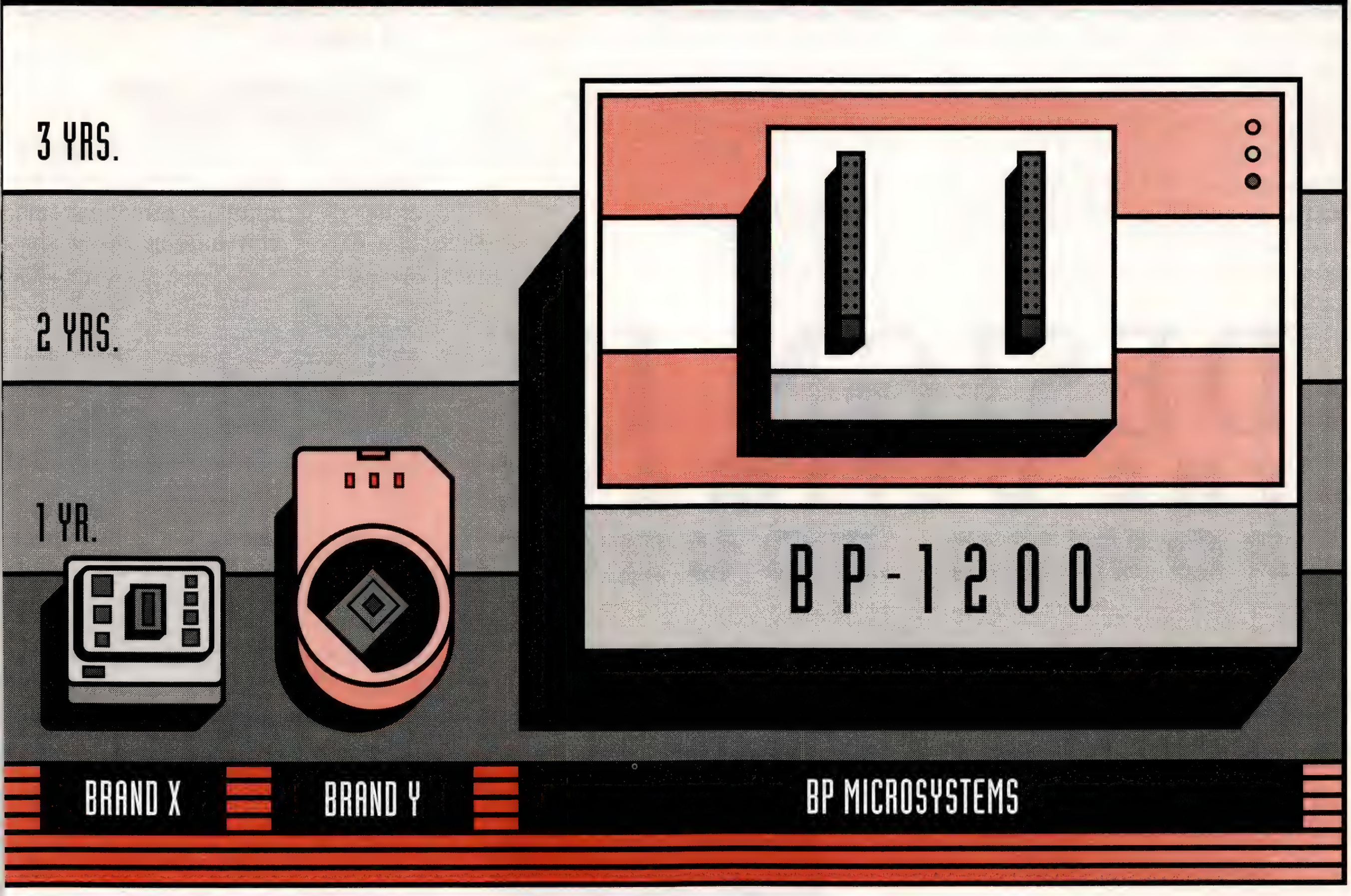

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▼ PCMCIA CARD COMBINES FAX, MODEM, AND VOICE

Designed specifically for notebook, palmtop, or pen-based computers, the Mercury card combines a send and receive fax, a data modem, and voice integration in a PCMCIA Type 2 form factor. Delivered with Windows-compatible voice-enabled software, the card features a sleep mode to conserve system battery life. A Y-connector offers one jack for a phone line and another for a telephone handset, which acts as the system's speaker and microphone. Group 3 fax is supported up to 9600 bits/s, and the data modem operates at 2400 bits/s. The Mercury card sells for $245.

MagicRAM Inc.
1850 Beverly Blvd.
Los Angeles, CA 90057
(213) 413-9999
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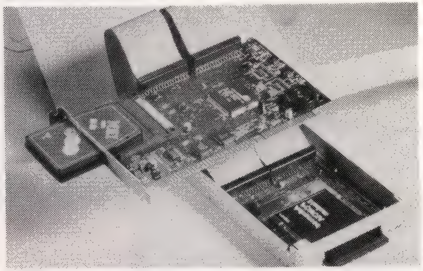

The CardPort family of PCMCIA-compatible drives are designed for either desktop or portable systems. The drives can handle cards that comply with the Type 1, 2, or 3 specifications. The CardPort eX, a self-contained unit, connects to the host computer through it's parallel port. The drive lasts several weeks on one charge. The CardPort is an internal module that plugs into a PC's backplane and supplies two card slots—one at the back of the board and one in a drive bay.

CNF Inc.
17705 Hale Ave., Bldg. I
Morgan Hill, CA 95037
(408) 778-1160
▶ **CIRCLE 900**

▼ 20-IN. X TERMINAL OFFERS 33-MHZ R3000 CPU

The CE and ME series X terminals are built with a 33-MHz R3000-compatible microprocessor. The PX20CE2 comes with a 20-in. color display with a resolution of 1280 by 1024 pixels. It boasts a performance rating of over 100,000 Xstones. Memory configurations range from 4 to 52 Mbytes, in 1-, 4-, or 16-Mbyte increments. There's also room for 2 Mbytes of PROM and 2 Mbytes of flash memory. The flash supplies a plug-and-play solution, because X-server software can be preloaded in the system. Available now, the PX20CE2 X terminal sells for $3495. With a 20-in. Trinitron CRT, it costs $3995.

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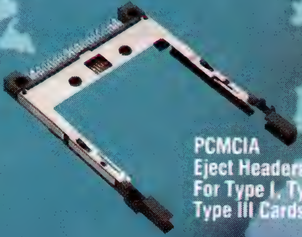

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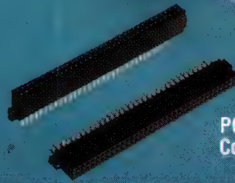

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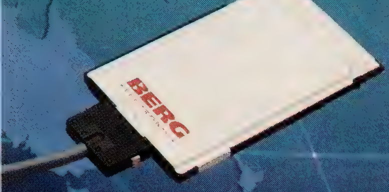

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DESIGN MAY NOT BE THE
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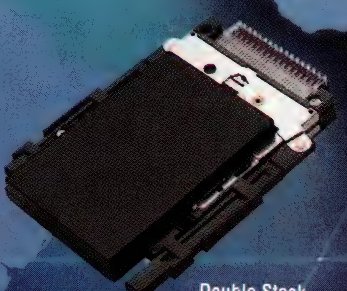

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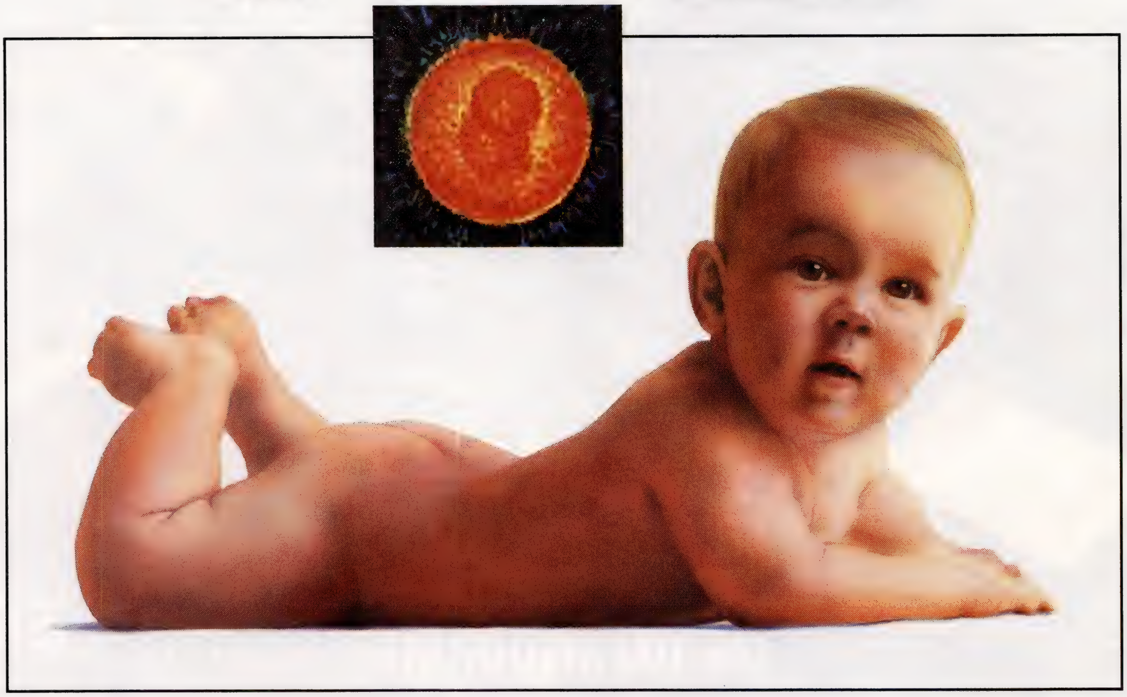

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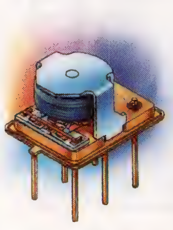

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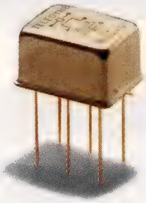
The A150 Attenuator Relay is housed in Teledyne Relays' extended Centigrid® hermetically sealed package. The two rows of connecting leads are 0.200″ apart and the leads are spaced 0.150″ center-to-center. It also features internal welded construction and uni-frame design for high motor magnetic efficiency and exceptional mechanical ruggedness. Its gold-plated precious metal contacts assure low contact circuit losses and reliable switching.

The A150 is the only RF Attenuator of its kind. For price, delivery and technical information, call **1-800-284-7007** or FAX us at 1-213-779-9161.



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CIRCLE 209 FOR U.S. RESPONSE **CIRCLE 210 FOR RESPONSE OUTSIDE THE U.S.**

A SPECIAL EDITORIAL FEATURE

PIPS

POWER • INTERCONNECTIONS • PASSIVES • SWITCHES • RELAYS

ELECTRONIC DESIGN

Fine-Pitch Packages Suit Interface ICs

Lower pin inductances and less ground bounce mean faster, quieter circuits.

BY MARK MUEGGE

Quality Semiconductor Inc., 851 Martin Ave., Santa Clara, CA 95050-2903; (408) 450-8000.

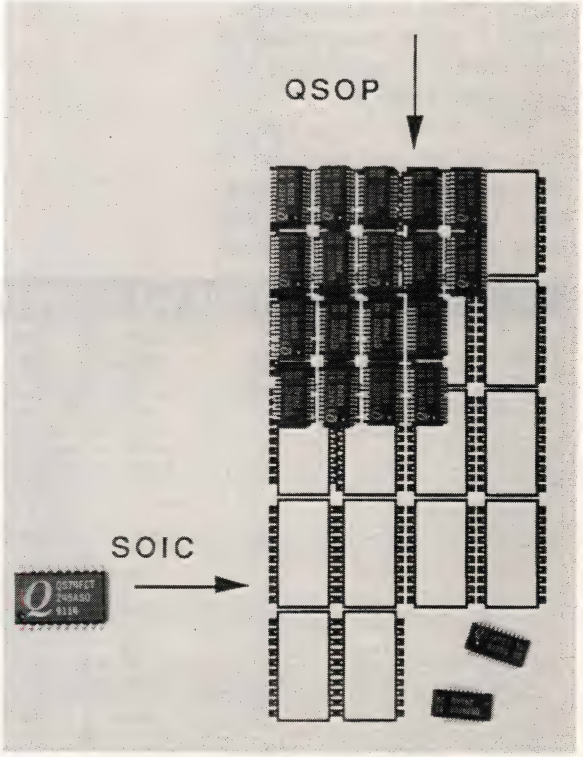
The relentless push to boost the performance of high-speed microprocessor-based systems demands that signal delays and noise, both on and off the chip, be reduced to their lowest levels. To a large extent, the packaging of devices can provide the answer to this growing problem. In recent years, packaging advances have significantly diminished signal delays and noise by bringing components closer together and by slashing their pin capacitances and inductances. Furthermore, improved lithography techniques continue to reduce signal delays and noise on the chip through performance gains and size reductions.

Shorter signal traces result in shorter delays and, therefore, faster signal speeds between system components. Every inch of trace on a 50-Ω circuit board costs about 150 ps, so it's critical that trace lengths are reduced in high-performance systems. Packaging advances such as the quad flat pack (QFP) have improved the performance of large pin-count devices, while fine-pitch packaging has similarly enhanced interface-logic devices. Moreover, buffers, transceivers, latches, and registers used to connect system blocks together have seen many recent packaging improvements.

Besides saving space, fine-pitch packages are also the quietest and fastest around. Smaller physical size means lower values of pin inductance and capacitance. And low pin inductance makes for a better connection to the circuit-board ground, which attenuates ground bounce. Ground bounce is noise coupled onto a non-switching output by other switching outputs. Improvements in circuit density and performance are due in large part to advances in fine-pitch packaging for interface-logic devices.

The first fine-pitch package for interface logic was the 300-mil-wide plastic small-outline IC (SOIC), also known as the small-outline package (SOP). The leads are formed in a gull-wing shape away from the body. The package's pin pitch is 50 mils and the board area required is about half that of the plastic dual in-line package (DIP). It enabled system designers to pack twice the amount of circuitry into the same area or pack the same amount of circuitry into half of the area.

Because the SOIC package is smaller than the DIP, its measured ground-lead inductance of 8.5 nH for the 20-pin version is almost half that of the 20-pin DIP (13.7 nH). Ground bounce is proportional to the square root of lead inductance, so the lower inductance means a 20% drop in ground bounce. While the SOIC's reductions in board area and noise generation are significant compared to the DIP, more recent gains in fine-pitch packaging for interface logic have gone farther.



Of all the standard production packages for interface logic, the 20- and 24-pin QSOPs have the smallest footprint. The body size is about one quarter of a standard SOIC package. The small package saves space and reduces noise without sacrificing thermal characteristics.

The smallest of the second-generation fine-pitch packages, however, are the 20- and 24-pin shrink SOPs (SSOPs). These packages are defined by lead pitches at or near 25 mils. Historically, two standards emerged for high-density packaging of interface logic at 20 and 24 pins. The Electronic Industry Association of Japan (EIAJ) endorsed a Japanese-developed, 208-mil-wide SSOP with a pin pitch of 25.6 mils (0.65 mm).

Meanwhile, in the United States, JEDEC endorsed a 150-mil-wide SSOP with a pin pitch of 25.0 mils (0.635 mm). This package, developed by Quality Semiconductor, is commonly referred to as the QSOP.

In addition to the QSOP and a 48-/56-pin SSOP, JEDEC has since endorsed the EIAJ-standard 20-/24-pin SSOP. The fact that JEDEC calls all of these packages SSOP can be confusing because of the proliferation of lead pitches and body widths. A chart comparing most of the packages used for interface logic can help allay some of that confusion *(Table 1)*. Another chart offers a quick comparison of lead pitches in metric and English units *(Table 2)*.

The 20- and 24-pin QSOPs have the smallest footprint of the standard production packages for interface logic. The body size is about one quarter of a standard SOIC package. The small package saves space while reducing noise without sacrificing thermal characteristics *(see the figure)*. The ground-lead inductance is 3.6 nH, which cuts ground bounce by 50% compared with the DIP. Thermal characteristics are excellent because of the high leadframe-to-plastic ratio, thus providing better heat conduction. The QSOP has gained wide acceptance in the industry, in part because it's based on the 14-pin narrow SOIC body.

The 20- and 24-pin SSOPs are also exceptionally small. In fact, other than the QSOP, no other standard package comes close to providing the board density of the low-pin-count SSOPs. The small size provides excellent noise reduction as well. Moreover, the SSOP has become widely accepted.

Drawbacks for these small packages are few. There's usually a slightly higher cost for the value-added features, such as space savings. Also, the false perception remains that more system components mean lower reliability. In fact, system reliability is more a function of total pin count rather than component count. The total pin count of two SSOPs is actually less than the 48- and 56-pin SSOPs for the same function.

The 48- and 56-pin SSOPs provide a space savings of 50% compared with the 24-pin SOIC package. The ground-lead inductance of the package is equivalent to the SOIC. Because devices assembled in these packages often have multiple ground pins, the effective ground-lead inductance, and resulting ground bounce, is on a par with the smallest packages. The thermal characteristics of the 48- and 56-pin SSOPs are favorable

TABLE 1: A COMPARISON OF INTERFACE-LOGIC PACKAGES

Package	Pin pitch	Length	Body width	Total width*	Package area (mm^2)	Equivalent board area (mm^2)**	Height	L_{GND} (e) = estimated	θ_{JA}*** (°C/W)
48 QVSOP	0.40 mm	10.0 mm	3.9 mm	6.2 mm	62.0	31.0	1.75 mm	3.0 nH (e)	86
20 TSSOP	0.65 mm	6.8 mm	4.4 mm	6.7 mm	45.6	45.6	1.1 mm	N/A	N/A
48 TSSOP	0.50 mm	12.8 mm	6.1 mm	8.4 mm	107.5	53.8	1.1 mm	N/A	115
20 QSOP	0.635 mm	0.344 in.	0.157 in.	0.244 in.	54.1	54.1	0.069 in.	3.6 nH	79
24 QSOP	0.635 mm	0.344 in.	0.157 in.	0.244 in.	54.1	54.1	0.069 in.	3.6 nH	70
24 TSSOP	0.65 mm	8.1 mm	4.4 mm	6.7 mm	54.3	54.3	1.1 mm	N/A	N/A
56 TSSOP	0.50 mm	14.3 mm	6.1 mm	8.4 mm	120.1	60.1	1.1 mm	N/A	115
20 SSOP	0.65 mm	7.5 mm	5.3 mm	8.2 mm	61.5	61.5	2.0 mm	N/A	112
24 SSOP	0.65 mm	8.5 mm	5.3 mm	8.2 mm	69.7	69.7	2.0 mm	N/A	94
48 FP	0.635 mm	15.6 mm	9.75 mm	N/A	152.1	76.0	2.18 mm	N/A	70
20 LCC	0.050 in.	0.358 in.	0.358 in.	N/A	82.7	82.7	0.090 in.	N/A	60
48 SSOP	0.635 mm	0.630 in.	0.299 in.	0.420 in.	170.7	85.4	0.110 in.	8.5 nH (e)	80
56 FP	0.635 mm	18.1 mm	9.75 mm	N/A	176.5	88.2	2.18 mm	N/A	60
56 SSOP	0.635 mm	0.730 in.	0.299 in.	0.420 in.	197.8	98.9	0.110 in.	8.5 nH (e)	80
20 FP	0.050 in.	0.540 in.	0.300 in.	0.305 in.	106.3	106.3	0.090 in.	N/A	110
28 LCC	0.050 in.	0.458 in.	0.458 in.	N/A	135.3	135.2	0.090 in.	N/A	50
20 SOIC	0.050 in.	0.510 in.	0.300 in.	0.416 in.	136.9	136.7	0.104 in.	8.5 nH	87
24 SOIC	0.050 in.	0.612 in.	0.300 in.	0.416 in.	164.3	164.3	0.104 in.	8.5 nH	75
24 FP	0.050 in.	0.640 in.	0.420 in.	0.440 in.	181.7	181.7	0.090 in.	N/A	100

- All values are maximum values
- Devices registered by JEDEC after 1991 use metric dimensions
- 25.4 mm/in. used for conversion between English and metric units

* Total width package includes leads
** Normalized to 8-bit-wide function (double package areas are divided by 2)
*** No air flow
N/A = not available

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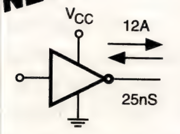

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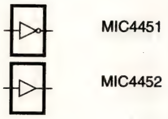

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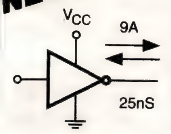

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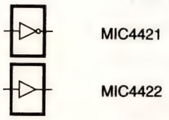
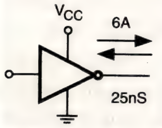
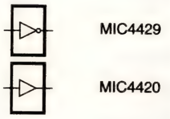
- Withstands 5V Negative Swing
- Surface Mount and High Power Package Available

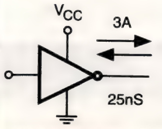




Drives a hex 6—hex 7 size
MOSFET; 1500pF—16,000pF

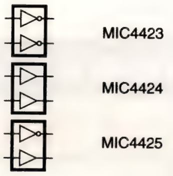
MIC4420/4429
- 6A Peak Output
- 2.5Ω Output Impedance
- 4.5V to 18V Supply
- 25nS into 2500pF
- Latch-up Protected
- Withstands 5V Negative Swing
- Surface Mount and High Power Package Available

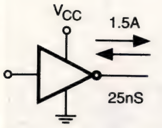




Drives a hex 4—hex 5 size
MOSFET; 600pF—12,000pF

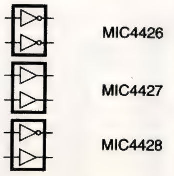
MIC4423/4424/4425
- 3A Peak Output
- 3.5Ω Output Impedance
- 25nS into 1800pF
- 4.5V to 18V Supply
- Latch-up Protected
- Withstands 5V Negative Swing
- Surface Mount Available

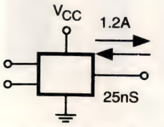




Drives a hex 0—hex 3 size
MOSFET; 400pF—3000pF

MIC4426/4427/4428
- 1.5A Peak Output
- 7Ω Output Impedance
- 25nS into 1000pF
- 4.5V to 18V Supply
- Latch-up Protected
- Withstands 5V Negative Swing
- Surface Mount Available





Drives a hex 0—hex 3 size
MOSFET; 400pF—3000pF

MIC4467/4468/4469
- 1.2A Peak Output
- 10Ω Output Impedance
- 25nS into 470pF
- 4.5V to 18V Supply
- Latch-up Protected
- Withstands 5V Negative Swing
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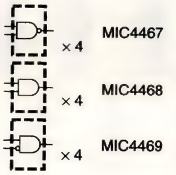

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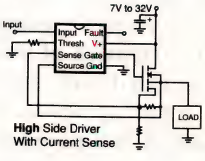

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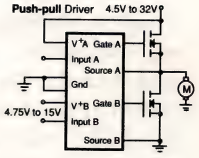
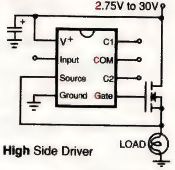
  MIC5011 Minimum Parts Count



MIC5012

NEW



MIC5014

MIC5014 Family
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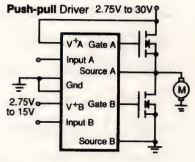

MIC5016

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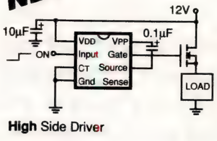

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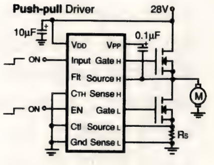

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because of their relatively large amount of leadframe material, which conducts more heat.

In some applications, it's as important to reduce package height as it is to reduce package length and width. In such cases (including disk-drive and PCMCIA circuits), the package of choice is the thin shrink small-outline package (TSSOP). These packages are only 1.1 mm thick—less than half the thickness of the standard SOIC package. The TSSOP packages come in 20 and 24 pins for standard interface logic and 48 and 56 pins for double-width logic.

The 20-pin TSSOP is the smallest package available for standard-width interface logic and, like the QSOP, uses about one-quarter of the board area of the SOIC package. While the advantages provided by these new thin packages can be enormous, there are trade-offs to consider. For example, system designers need to understand the thermal characteristics of these packages so that any potential problem with localized-device power dissipation can be avoided during board layout.

Other than board area, the most important design consideration in choosing a package is thermal resistance. Thermal resistance is a measure of a package's ability to conduct heat away from the die to the outside world. Lower thermal resistance means lower die temperatures and, hence, higher reliability.

The most common thermal-resistance parameter used by designers today is θ_{JA}. This is a measure of the thermal resistance between the junction temperature of the silicon and the ambient temperature, and is expressed in °C/W. To determine θ_{JA}, a special test die is used to measure the temperature inside the package. The difference between the die temperature and ambient temperature is then divided by the amount of power used by the die. The lower the package's θ_{JA}, the better that package is at conducting heat away from the IC.

TABLE 2: PIN-PITCH CONVERSION

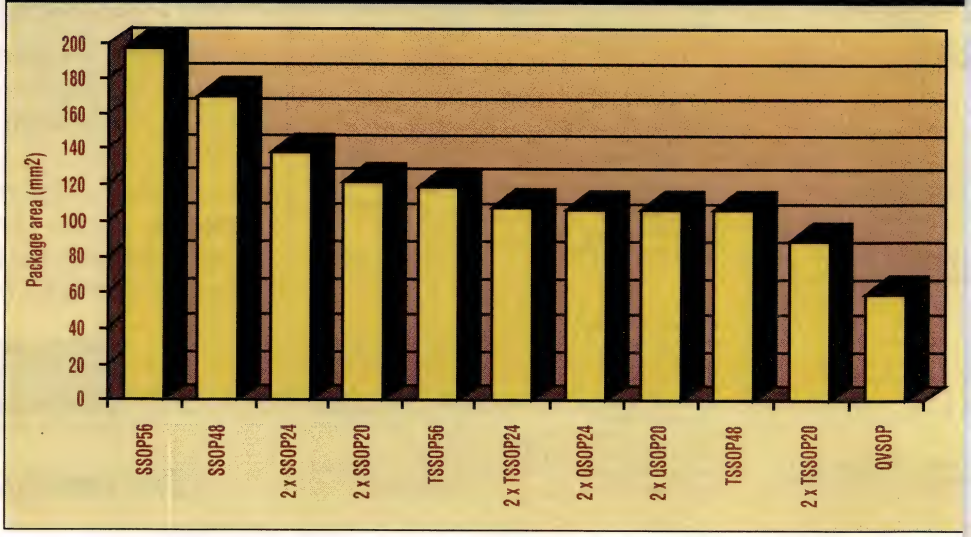
English units	Metric units
50 mils	1.27 mm
25.6 mils	0.65 mm
25.0 mils	0.635 mm
19.7 mils	0.5 mm
15.7 mils	0.4 mm

Many packaging parameters affect thermal resistance. The most critical of these are the size of the die-attach pad (and associated die size) and the ratio of leadframe material to plastic. A larger die-attach pad (with a larger die) usually means a more even distribution of heat generated by the device. Such conditions generally favor heat conduction and result in lower thermal resistance. A greater proportion of leadframe material relative to the amount of plastic also results in better thermal characteristics. Again, this allows more efficient conduction of heat away from the die. Other parameters that can affect thermal resistance are the leadframe material itself and the leadframe's design.

One area that's been largely ignored in terms of package development for interface logic is the military market. Perhaps IC manufacturers are concerned about the military's current trend toward downsizing, translating into less long-term business. This flies in the face of current indications suggesting that while the overall military piece of the pie is shrinking, the electronics industry's slice is growing. To take advantage of this trend, newer and more efficient packages for the military interface-logic market must be developed. There have been packaging advances for larger-pin-count devices, such as a ceramic version of the QFP and a 32-pin ceramic SOIC for memories, but new military packages for interface logic are nonexistent.

To date, the ceramic leadless chip carrier (LCC) and ceramic flat packs have been the only options available for surface-mount users of interface logic in the military market. Both packages possess contacts or leads spaced at 50 mils. And, both use significantly less board space than the ceramic DIP package. However, neither are without drawbacks. The LCC package can pop off of boards because of thermal or mechanical stress. Because the package has no leads, it's more difficult to ensure a highly reliable solder joint. To eliminate this problem, designers have actually soldered leads onto the LCC package before soldering onto the board to

TABLE 3: A COMPARISON OF PACKAGE AREAS FOR DOUBLE-WIDTH LOGIC



guarantee a better joint. Of course, this additional processing adds expense and time to the board-manufacturing process.

Flat packs occupy less space than ceramic DIPs and, because they are leaded, it's easier to ensure a high-reliability solder joint. The flat pack is typically shipped from the manufacturer to the user in plastic carriers. These carriers protect the unformed leads during the manufacturing process. The carriers must be removed and the leads trimmed and formed before the device can be placed and soldered on the board. As such, flat packs require some additional processing by the user and are generally much more expensive than the LCC package.

The ceramic SOP package lends several advantages to interface logic. For instance, the package would cost significantly less than flat packs, for both suppliers and users. Less handling would be required, because much of the same equipment used for the plastic SOP still applies. The ceramic SOP takes less board area than do flat packs, and the footprint is compatible with that of the plastic SOP. This key feature would cut prototyping costs for military systems and would enable plastic SOPs to replace the ceramic SOPs in commercial versions of the same circuits without requiring a re-layout of the circuit board. Unfortunately, ceramic SOPs have yet to be developed for interface logic. However, given the strong need for such a package, a solution is no doubt on the horizon.

The state of the art in interface-logic packaging is in pin pitches below 0.5 mm. The JEDEC-registered 48-pin QVSOP package offers the highest density of any interface-logic package *(Table 3)*. It's over five times smaller than the SOIC package for the same function. The space savings is achieved by implementing a leadframe with a 0.4-mm pitch and using the body from the 16-pin narrow SOIC. This same pitch is used by large pin-count packages like the shrink quad flat pack (SQFP).

The combination of fine pitch and narrow body results in excellent thermal characteristics and low ground bounce. The high ratio of metal to plastic gives a thermal resistance of only 86°C/W. Thanks to the package's relatively low ground-lead inductance of 3.0 nH, ground bounce is reduced by 35% compared with an SOIC. When two ground pins are used for each 8 bits, the effective ground bounce is almost cut in half. As a result, ground bounce is cut by an additional 25%.

System performance can be greatly improved by using fine-pitch packaging for interface logic. These gains are realized through shorter trace lengths on circuit boards and by lower pin inductances, ultimately diminishing ground bounce. The first of the fine-pitch packages, the SOIC, provided a large improvement over the DIP. The next package generation, the SSOPs, realized a quantum-leap improvement beyond previous generations. These 25-mil pin-pitch packages are the state of the art in volume manufacturing for interface-logic devices. Packaging for interface logic has also branched out into specialty applications requiring very thin packaging, which has been serviced by the TSSOP packages. For the highest-density applications, the QVSOP package is the smallest available for interface logic.

Mark Muegge, a senior applications engineer at Quality Semiconductor Inc., holds a BSEE from the University of California, Davis. Muegge joined QSI in 1989.

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Hysol Engineering Adhesive
One Dexter Dr.
Seabrook, NH 03874-4018
(603) 474-5541
(EN) (EA) (PM)
CIRCLE 648

Digital Equipment Corp.
4 Results Way, MR04-3/C19
Marlboro, MA 01752
(508) 467-3394
(BM) (CN) (CM) (EM) (GP) (IN) (MP) (PT) (RA) (VR) (WT)
CIRCLE 649

Dow Chemical Co.
Dow Plastics Div.
P.O. Box 1206
Midland, MI 48641-1206
(800) 441-4DOW
(EP) (EA) (RE)
CIRCLE 650

Du Pont Electronic Materials
Barley Mill Plaza
Room G-52198
Wilmington, DE 19880-0010
(919) 248-5075
(CE) (IK) (TF)
CIRCLE 651

Dymax Corp.
51 Greenwoods Rd.
Torrington, CT 06790
(203) 482-1010
(CC) (EN) (EA) (LA) (PM) (SA)
CIRCLE 652

E-A-R Specialty Composites
7911 Zionsville Rd.
Indianapolis, IN 46268
(317) 692-1111
(GK) (EL) (SA)
CIRCLE 653

ECS Composites Inc.
3560 Rogue River Hwy.
Grants Pass, OR 97527
(503) 476-8872
(CN) (CM) (EM) (GP) (IN) (MI) (PT) (RA) (WT) (ES) (ER)
CIRCLE 654

EG&G Wakefield Engineering
60 Audubon Rd.
Wakefield, MA 01880
(617) 245-5900
(BM) (CM) (GP) (IN) (MP) (RA) (EA)
CIRCLE 655

EMCA-REMEX Products
Ablestik Electronic Materials
160 Commerce Dr.
Montgomeryville, PA 18936
(215) 855-1000
(IK) (MM) (PC) (TF)
CIRCLE 656

EPH Engineering Assoc. Inc.
21 E. 400 S. St.
Orem, UT 84058
(801) 226-1383
(MP) (CE) (SU)
CIRCLE 657

ERNI Components
520 Southlake Blvd.
Richmond, VA 23236
(804) 794-6367
(GP)
CIRCLE 658

ESP Inc.
14 Blackstone Valley Pl.
Lincoln, RI 02865-1145
(800) 338-4353
(FL) (SO)
CIRCLE 659

(see p. 146 for key)

(continued on p. 136)

▼ TAPING PRODUCTS OFFER INSULATION

A self-fusing, "no-heat" silicone tape and a moldable rubber tape are both available for waterproofing and insulating applications. The Type TYT200 silicone tape is self-adhering and fuses to form a homogeneous mass within 24 hours at room temperature and in four hours at 350°F. Type TYT250 is a waterproofing moldable-rubber tape that may be shaped or pressed in place and conforms to the space, shape, or joint being filled. Pricing in small quantities is $17.85/roll for Type TYT200 and $12.15/roll for Type TYT250.

Cole-Flex
91 Cabot St.
West Babylon, NY 11704
(516) 249-6150
▶CIRCLE 824

▼ VERSATILE RACK HOUSES SYSTEMS

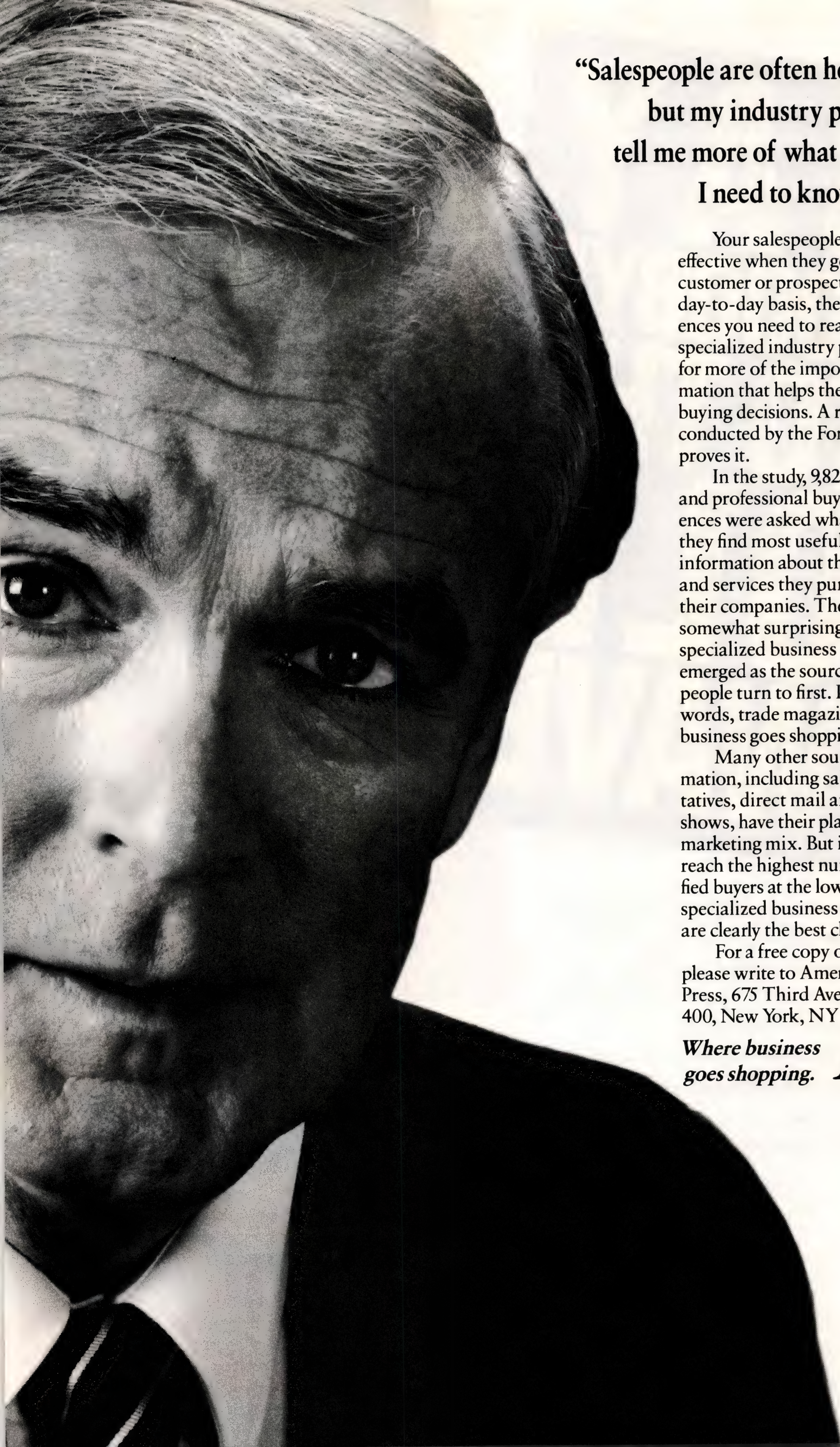
The Miracel multi-use industrial electronics rack is imbued with engineering features that enhance its versatility and ease of use. For example, the units' doors can be opened 180° in stand-alone or bayed-together versions. Also, the doors can be removed and/or reorientated from left- to right-hand hinging by one person. Metric and 19-in. components can be installed in dedicated or hybrid enclosures. A comprehensive range of accessories is available.

Knurr USA Inc.
1890 N. Voyager Ave.
Simi Valley, CA 93063
(805) 526-7733
▶CIRCLE 825

▼ POTTING COMPOUND COOLS COMPONENTS

A thermally conductive, electrically insulating epoxy system is available for casting, potting, and encapsulation applications. The EP30AO system cures at room temperature or more rapidly at elevated temperatures. It offers an exceptionally low viscosity and can be cast or potted in variable cross-section thicknesses. Shrinkage after curing is minimal. Call for pricing and delivery.

Master Bond Inc.
154 Hobart St.
Hackensack, NJ 07601
(201) 343-8983
▶CIRCLE 826



"Salespeople are often helpful, but my industry publications tell me more of what I need to know."

Your salespeople can be effective when they get to see a customer or prospect. But, on a day-to-day basis, the buying influences you need to reach turn to specialized industry publications for more of the important information that helps them make buying decisions. A recent study, conducted by the Forsyth Group, proves it.

In the study, 9,823 business and professional buying influences were asked what sources they find most useful in providing information about the products and services they purchase for their companies. The results were somewhat surprising. Overall, specialized business publications emerged as the source business people turn to first. In other words, trade magazines are where business goes shopping.

Many other sources of information, including sales representatives, direct mail and trade shows, have their place in the total marketing mix. But if you want to reach the highest number of qualified buyers at the lowest cost, specialized business publications are clearly the best choice.

For a free copy of the study, please write to American Business Press, 675 Third Avenue, Suite 400, New York, NY 10017.

Where business goes shopping. ABP

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CIRCLE 173 FOR U.S. RESPONSE

CIRCLE 174 FOR RESPONSE OUTSIDE THE U.S.

▼ THIN-FILM PROCESS OFFERS 2-MIL SPACING

Thin-film processing that allows 2-mil line spacing, as opposed to 4-mil spacing that's possible with thick films, is provided by Kyocera America Inc.'s San Diego facility. The company's high-temperature applicable thin-film processing also permits brazing at up to 850°C with copper-silver for attachment of leads or components. Such brazing provides for improved pin or lead stability and strength during die attach compared with standard soldering. It can be performed on multilayer or cofired metallized packages for better adhesion of thin-film metallization. Call for pricing and delivery.

Kyocera America Inc.
Thin Film Div.
8611 Balboa Ave.
San Diego, CA 92123-1580
(619) 576-2600
▶CIRCLE 827

▼ FLEXIBLE CABINETS FILL SPECIAL NEEDS

Cabinet needs, from standard configurations to custom requirements, can be filled without added cost or long waits by the Zero Guardian extra-duty cabinets. The Guardian cabinets can be designed in virtually any size and configuration in either steel or aluminum to solve special, and even severe, packaging requirements. The units' rugged welded construction and test-proven standards compliance ensures their capabilities in EMI shielding and resistance to shock, moisture, fungus, and temperature extremes. Delivery is in from one to six weeks. Call for pricing.

Zero Corp.
Zero East Div.
P.O. Box 128
Monson, MA 01057-0128
(413) 267-5561
▶CIRCLE 828

▼ DESKTOP ENCLOSURE HOUSES CPUs

The latest addition to a line of injection-molded PC housings is the ATLC Series of desktop CPU enclosures. The units combine contemporary styling with improved EMI-shielding properties. Several integrator-friendly features include quick, "one-screw" disassembly; a snap-out front bezel; and easy access for internal and external disc-drive mounting. Available with a 200-W power supply, the enclosures also have a second-fan option for Pentium-based systems. In addition, an optional conversion from desktop to mini-tower configuration is available. Call for pricing and delivery data on all models and options.

Palo Alto Design Group Inc.
360 University Ave.
Palo Alto, CA 94301
(415) 327-9444
▶CIRCLE 829

PACKAGING AND MATERIALS MANUFACTURERS

Electrical Insulation Suppliers
300 N. Mannheim Rd.
Hillside, IL 60162
(708) 547-5400
(ES) (ER) (FR) (GK) (MG) (RC) (SE) (TB) (VE) (WN) (CC) (EL) (EN) (EP) (EA) (PF) (FP) (FE) (FL) (IK) (LA) (MM) (MC) (PC) (PM) (RE) (SA) (SO) (SU) (TF)
CIRCLE 660

Electro Insulation Corp.
3921 Ventura Dr.
Arlington Heights, IL 60004-7952
(708) 632-1020
(BM) (TB) (CC) (FE) (SO)
CIRCLE 661

Electro-Science Labs Inc.
416 E. Church Rd.
King of Prussia, PA 19406-1533
(215) 272-8000
(EN) (PC) (SA) (TF)
CIRCLE 662

Electro-Space Fabricators Inc.
300 W. High St.
Topton, PA 19562-0067
(215) 682-7181
(CN) (CM) (EM) (GP) (MI) (RA) (VR)
CIRCLE 663

Electronic Solutions
Scanbe
6790 Flanders Dr.
San Diego, CA 92121
(619) 452-9333
(BM) (CM) (EM) (GP) (MP) (MI) (RA) (ER) (GK)
CIRCLE 664

Electrorack Products Co.
1443 S. Sunkist St.
Anaheim, CA 92806
(714) 776-5420
(CN) (EM) (IN) (RA) (VR) (WT) (ES) (ER) (GK) (WN)
CIRCLE 665

Elf Atochem Sensors Inc.
Piezo Film Sensors Div.
950 Forge Ave.
Norristown, PA 19403
(215) 666-3505
(PF)
CIRCLE 666

Elma Electronic Inc.
44350 Grimmer Blvd.
Fremont, CA 94538
(510) 656-3400
(BM) (CN) (CM) (EM) (GP) (IN) (PT) (RA) (VR) (WT) (ER)
CIRCLE 667

Emerson & Cuming Inc.
Div. of W.R. Grace & Co.
77 Dragon Ct.
Woburn, MA 01888
(800) 832-4929
(CC) (EN) (EA) (IK) (PM)
CIRCLE 668

Enclosure Technologies Inc.
256 Airport Industrial Dr.
Ypsilanti, MI 48198
(313) 481-2200
(BM) (CN) (CM) (GP) (IN) (RA) (VR)
CIRCLE 669

Enthone-OMI Inc.
P.O. Box 1900
New Haven, CT 06508
(203) 799-4904
(ER) (FL)
CIRCLE 670

Epoxy Technology Inc.
14 Fortune Dr.
Billerica, MA 01821
(508) 667-3805
(EN) (EA) (PM)
CIRCLE 671

Equipto Electronics Corp.
351 Woodlawn Ave.
Aurora, IL 60510
(708) 897-4691
(CN) (CM) (EM) (IN) (MI) (RA) (VR) (ER)
CIRCLE 672

Everest Electronic Equipment
2100 E. Orangewood Ave.
Anaheim, CA 92806
(714) 634-2866
(BM) (CN) (CM) (EM) (IN) (PT) (RA) (VR)
CIRCLE 673

Ferro Corp.
Electronic Materials Div.
27 Castilian Dr.
Santa Barbara, CA 93117-3092
(805) 968-5000
(CE) (IK) (PC) (TF)
CIRCLE 674

Flex Products Inc.
2793 Northpoint Pkwy.
Santa Rosa, CA 95407
(707) 525-7926
(ER) (LA)
CIRCLE 675

Frenchtown Ceramics Co.
8th & Harrison St.
Frenchtown, NJ 08825
(908) 996-2121
(CM) (MI) (CE)
CIRCLE 676

Fujipoly Inc.
750 Walnut Ave.
Cranford, NJ 07016
(908) 272-3850
(SE) (TB) (EL) (SA)
CIRCLE 677

Fujitsu Components of America
Component Div.
3545 N. First St.
San Jose, CA 95054
(408) 922-9000
(ER)
CIRCLE 678

GE Plastics
One Plastics Ave.
Pittsfield, MA 01201
(800) 845-0600
(EL) (EP) (FP) (RE)
CIRCLE 679

GE Silicones
260 Hudson River Rd.
Waterford, NY 12188
(518) 233-3550
(CC) (EL) (EN) (EA) (PM) (RE) (SA)
CIRCLE 680

Gardiner Metal Co.
4820 S. Campbell Ave.
Chicago, IL 60632
(312) 847-0100
(FL) (SO)
CIRCLE 681

General Devices Co. Inc.
P.O. Box 39100
Indianapolis, IN 46239
(317) 897-7000
(CN) (CM) (EM) (GP) (MI) (PT) (RA) (VR)
CIRCLE 682

Glasteel Industrial Laminates
P.O. Box 910
Collierville, TN 38027
(901) 853-5070
(LA)
CIRCLE 683

Glenmarc Mfg. Inc.
2404 Spring Ridge Dr., Unit D
Spring Grove, IL 60081
(815) 675-1080
(EL) (EN) (EA) (PM)
CIRCLE 684

Graseby Plastic Systems Inc.
261 Cedar Hill St.
Marlboro, MA 01752
(508) 485-7390
(ES)
CIRCLE 685

Heraeus Inc.
Cermalloy Div.
24 Union Hill Rd.
West Conshohocken, PA 19428
(215) 825-6050
(EA) (FL) (IK) (SO) (TF)
CIRCLE 686

Hirose Electric USA Inc.
2685-C Park Center Dr.
Simi Valley, CA 93065
(805) 522-7958
(ES) (ER) (FR)
CIRCLE 687

Hoechst Celanese Corp.
Advanced Materials Group
26 Main St.
Chatham, NJ 07928
(201) 635-4198
(RE)
CIRCLE 688

(see p. 146 for key)
(continued on p. 138)

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CIRCLE 249 FOR U.S. RESPONSE **CIRCLE 250 FOR RESPONSE OUTSIDE THE U.S.**

PACKAGING & MATERIALS

▼ EMI/RFI GASKET CUTS INSTALLED COST

A significant reduction in the overall cost of electromagnetic shielding gaskets is offered by the Peel 'n Shield system. The gaskets are claimed as the first to use automated production techniques to reduce both material and labor content of an installed EMI/RFI shield while still providing shielding effectiveness through 100 dB. A carrier and release sheet system allows easy and precise positioning of gaskets on their intended surface. Call for pricing and delivery.

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555 Paper Mill Rd.
Newark, DE 19714
(800) 231-4364
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▼ NO-CLEAN SOLDER IS FREE OF HALIDES

A solder cream tolerates a wide range of process conditions and is formulated for high-reliability applications. The halide-free NC40 solder cream leaves a minimum of residues, making automatic pin testing feasible without cleaning. Any residues that do remain are clear, inert, and fall within the SIR and electromigration requirements of Bellcore and IPC. An advanced solvent blend gives extended open time on screen printers. Call for pricing and delivery information.

Multicore Solders Inc.
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(214) 238-1224
▶ CIRCLE 831

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Over 1200 standard sizes are available in a line of MIL-SPEC watertight aluminum cases. Special sizes are also available without tooling charges. All transit and combination cases are designed to meet MIL-STD-108 or MIL-T-28800. Enclosures are available with dual covers, shock-mount isolation, and a variety of other options. Hinged compartments are available in covers for storage of manuals, cables, or spare parts. Delivery is in four to six weeks. Call for pricing.

Instrument Enclosures
4088 South K St.
Tulare, CA 93274
(209) 688-1100
▶ CIRCLE 832

PACKAGING AND MATERIALS MANUFACTURERS

Hoffman Engineering Co.
900 Ehlen Dr.
Anoka, MN 55303-7504
(612) 421-2240
(BM) (CN) (CM) (EM) (GP) (IN) (PT) (VR) (WT) (ER) (GK) (VE) (WN)
CIRCLE 689

HumiSeal
P.O. Box 445
Woodside, NY 11377
(718) 932-0800
(CC)
CIRCLE 690

Hybricon Corp.
12 Willow Rd.
Ayer, MA 01432
(508) 772-5422
(BM) (CM) (EM) (GP) (PT) (RA) (VR)
CIRCLE 691

I.M.R. Corp.
Micro Electronic Research
11132 E. Edison St.
Tucson, AZ 85749
(602) 749-1920
(MP) (ES) (ER) (CE) (CC) (EN) (EA) (IK) (PC) (PM) (TF)
CIRCLE 692

Imtec Inc.
One Imtec Lane
Bellows Falls, VT 05101
(802) 463-9502
(FP) (FE) (LA)
CIRCLE 693

Indium Corp. of America
1676 Lincoln Ave.
Utica, NY 13502
(315) 768-6400
(FL) (SA) (SO)
CIRCLE 694

Instrument Enclosures
4088 South K St.
Tulare, CA 93274
(209) 688-1100
(CM) (EM) (IN) (MI) (PT) (WT)
CIRCLE 695

Instrument Specialties Co. Inc
P.O. Box A, Broad St.
Delaware Water Gap, PA 18327-0136
(717) 424-8510
(ER) (GK) (SE) (TB) (VE)
CIRCLE 696

Interlogic Industries
85 Marcus Dr.
Melville, NY 11747
(516) 420-8111
(CM) (GP) (IN) (RA)
CIRCLE 697

International Electronic Research Corp.
135 W. Magnolia Blvd.
Burbank, CA 91502
(818) 842-7277
(CM) (MI)
CIRCLE 698

JMR Europe
19320 Londelius St.
Northridge, CA 91324
(818) 993-4801
(BM) (CM) (EM) (GP) (MI) (RA) (EP)
CIRCLE 699

Johnson Matthey Inc.
Electronics Div.
10080 Willow Creek Rd.
San Diego, CA 92131
(619) 566-9510
(EA) (IK) (TF)
CIRCLE 700

Keystone Electronics Corp.
31-07 20th Rd.
Astoria, NY 11105-2017
(718) 956-8900
(IN)
CIRCLE 701

Knurr USA Inc.
1890 N. Voyager Ave.
Simi Valley, CA 93063
(805) 526-7733
(BM) (CN) (CM) (EM) (IN) (MI) (PT) (RA) (VR) (WT) (ES) (ER)
CIRCLE 702

Kyocera America Inc.
Microelectronics Div.
1740 Technology Dr.
Suite 490
San Diego, CA 95110
(408) 437-8777
(CM) (MP) (CE)
CIRCLE 703

Langley Div.
Fleet Aerospace Co.
310 Evelid Ave.
San Diego, CA 92114
(619) 264-3181
(CN) (CM) (EM) (MI) (RA) (VR) (WT)
CIRCLE 704

Lanxide Electronic Components
1300 Marrows Rd.
Newark, DE 19714
(302) 456-6300
(MP) (MI) (RA) (MC)
CIRCLE 705

Lauren Mfg. Co.
2228 Reiser Ave. S.E.
New Philadelphia, OH 44663
(216) 339-3373
(GK) (EL)
CIRCLE 706

Lindgren RF Enclosures
400 High Grove Blvd.
Glendale Heights, IL 60139
(708) 307-7200
(CM) (EM) (PT) (ER) (MG) (RC) (VE) (WN)
CIRCLE 707

Loctite Corp.
North American Group
705 N. Mountain Rd.
Newington, CT 06111
(203) 278-1280
(EA)
CIRCLE 708

Lytron Inc.
55 Dragon Ct.
Woburn, MA 01801
(617) 933-7300
(RA)
CIRCLE 709

Magnetic Shield Corp.
740 N. Thomas Dr.
Bensenville, IL 60106
(708) 766-7800
(ER) (MG) (RC) (SE) (TB)
CIRCLE 710

Markel Corp.
P.O. Box 752
Norristown, PA 19404
(215) 272-8960
(TB)
CIRCLE 711

Master Bond Inc.
154 Hobart St.
Hackensack, NJ 07601
(201) 343-8983
(ER) (CC) (EN) (EA) (PM) (RE)
CIRCLE 712

Mereco Technologies
1505 Main St.
West Warwick, RI 02893
(401) 822-9300
(ER) (GK) (CC) (EL) (EN) (EA) (IK) (PM) (RE) (SA)
CIRCLE 713

Meritec
Div. of Associated Enterprises
1359 Jackson St.
P.O. Box 8003
Painesville, OH 44077
(216) 354-3148
(ER)
CIRCLE 714

Mideast Aluminum Industries
Route 130
Dayton, NJ 08810-0248
(908) 329-8000
(CM) (GP) (IN) (RA) (VR)
CIRCLE 715

Miller-Stephenson Chemical Co.
55 Backus Ave.
Danbury, CT 06810
(203) 743-4447
(ER) (CC) (EA) (RE)
CIRCLE 716

Minico
Div. of W.R. Grace Co.
50 N. Harrison Ave.
Congers, NY 10920
(914) 268-9120
(EA) (IK) (PC) (TF)
CIRCLE 717

Mitech Corp.
1780 Enterprise Pkwy.
Twinsburg, OH 44087
(216) 425-1634
(ES) (SE)
CIRCLE 718

Mobay
A Bayer USA Company
Plastics & Rubber Div.
Mobay Rd.
Pittsburgh, PA 15205-9741
(412) 777-3800
(EP)
CIRCLE 719

Monsanto Co.
The Chemical Group
800 N. Lindbergh Blvd.
St. Louis, MO 63167
(314) 694-2251
(EM) (MF) (ER)
CIRCLE 720

(see p. 146 for key)
(continued on p. 140)

You Need Tree City USA

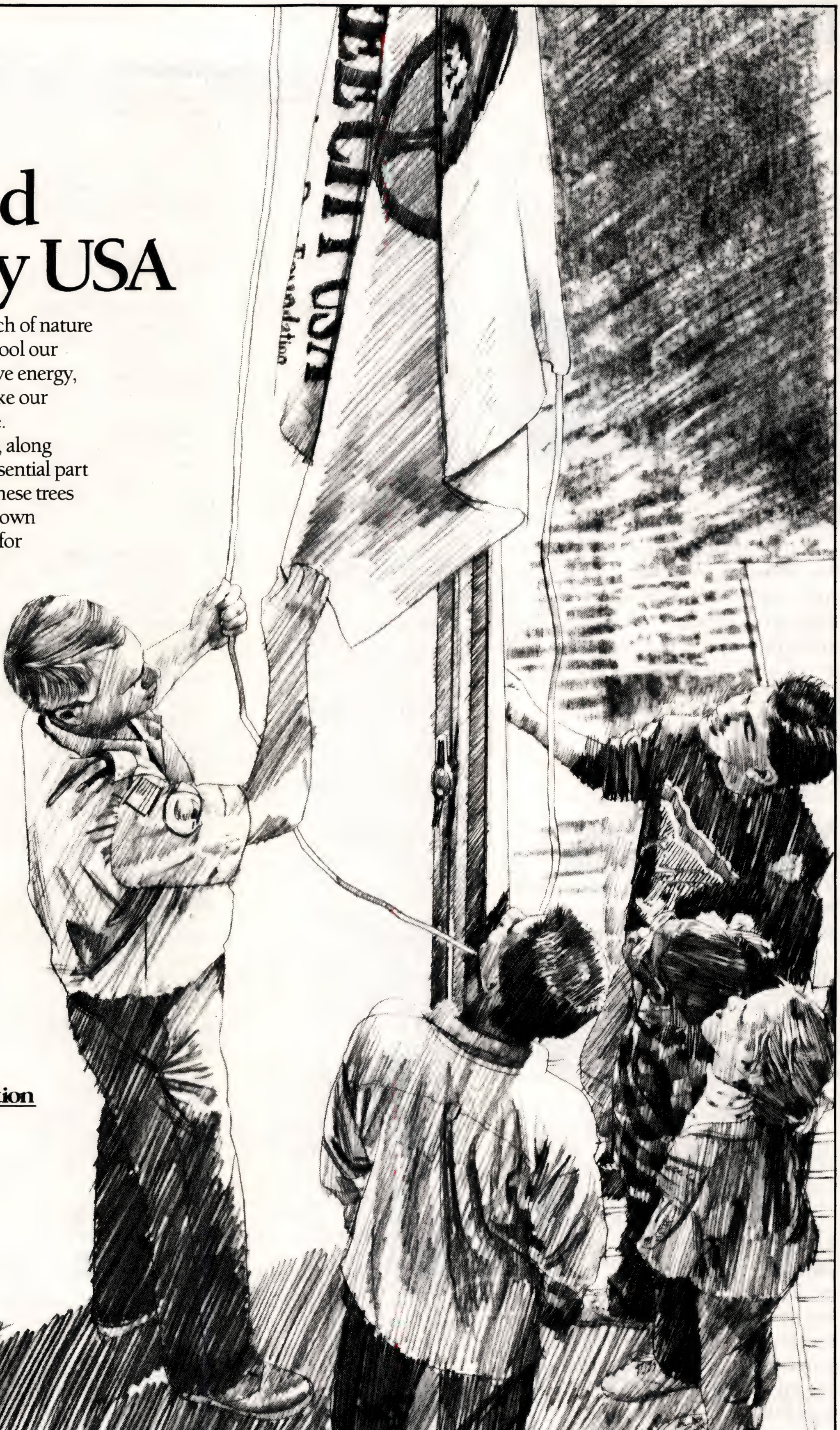
City trees add the soft touch of nature to our busy lives. They cool our cities, fight pollution, conserve energy, give wildlife a home, and make our neighborhoods more liveable.

The trees on city property, along streets and in parks, are an essential part of the urban forest. To keep these trees healthy and abundant, your town needs an organized program for their care... an annual action plan to plant and prune the city's trees, and to maintain their health.

You can make a difference — by planting and caring for trees in your yard and in your neighborhood, and by encouraging your city government's community forestry program.

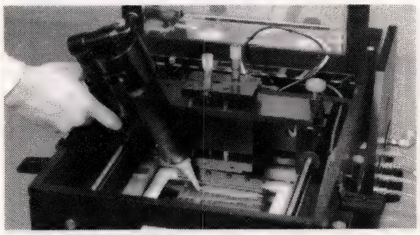
Support Tree City USA where you live. For your free booklet, write:
Tree City USA, The
National Arbor Day
Foundation, Nebraska
City, NE 68410.

The National Arbor Day Foundation



▼ ROBUST SOLDER CREAM IS WATER-SOLUBLE

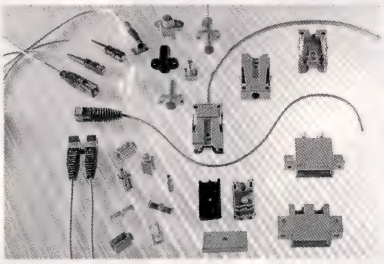
A robust, water-washable solder cream is available for standard and extra-fine-pitch stenciling and screening. The Series 400ADV cream is insensitive to heat, allowing drop-in substitution for existing water-soluble solders as well as RMA-based solders. Features include excellent brick definition and zero hot slump. Pitches from 50 to 12 mils can be screened without compromise, and screen life is 8 hours with no moisture pickup. Production quantities are shipped in three days from receipt of order. Call for pricing.



ESP
14 Blackstone Valley Pl.
Lincoln, RI 02865-1145
(800) 338-4353
▶ CIRCLE 833

▼ MOLDING COMPOUND SUITS FO CONNECTORS

The demanding materials requirements for a wide range of injection-molded fiber-optic connectors are met by Radel A polyethersulfone (PES) molding compound. The Fiber Optic Dept. at 3M's Telecom Systems Group, Eatontown, N.J., selected the material for its ability to support critical alignments in units of microns. In addition, the material meets Bellcore standards that involve a 30-day test with cycling between –40 and +85°C. Call for pricing and delivery.



Amoco Performance Products Inc.
4500 McGinnis Ferry Rd.
Alpharetta, GA 30202-3914
(404) 772-8200
▶ CIRCLE 834

PACKAGING AND MATERIALS MANUFACTURERS

Multicore Solders
1751 Jay Ell Dr.
Richardson, TX 75081
(214) 238-1224
(FL) (SO)
CIRCLE 721

Mupac Corp.
10 Mupac Dr.
Brockton, MA 02401
(508) 588-6110
(GP) (BM) (VR) (PT) (EM) (CM)
CIRCLE 722

NELCO
3 Elm St.
Walden, NY 12586
(914) 778-2111
(LA) (SU)
CIRCLE 723

NEPTCO Inc.
30 Hamlet St.
Pawtucket, RI 02861
(401) 722-5500
(ER) (FP) (FE) (LA) (SA)
CIRCLE 724

Norlabs
a Div. of R.H. Carlson Co.
41 Chestnut St.
Greenwich, CT 06830
(203) 531-5500
(CC) (EL) (EN) (EA) (PM) (RE)
CIRCLE 725

Olin Hunt Conductive Materials
1496 E. Francis St.
Ontario, CA 91761
(909) 947-2228
(ER) (TF)
CIRCLE 726

Omega Shielding Products Inc.
1384 Pompton Ave.
Cedar Grove, NJ 07009
(201) 890-7455
(ER) (GK) (MG) (SE)
CIRCLE 727

Optima EPS
2166 Mountain Industrial Blvd.
Tucker, GA 30084
(404) 496-4025
(CN) (CM) (EM) (IN) (MI) (PT) (RA) (VR) (WT) (ER) (GK)
CIRCLE 728

PFT Inc.
Hwy. 16 West
Monon, IN 47959
(800) 558-7297
(IN) (RA) (VR)
CIRCLE 729

PacTec
Div. of LaFrance Corp.
Enterprise & Executive Aves.
Philadelphia, PA 19153
(215) 365-8400
(GP) (IN) (PT) (EM) (CM) (ER)
CIRCLE 730

Pacific Microelectronics Corp.
10575 S.E. Cascade Blvd.
Portland, OR 92223
(800) 622-5574
(CM) (MP) (WT) (CE) (SU) (TF)
CIRCLE 731

Pacific West Enclosures
1370 Logan Ave., Suite A/B
Costa Mesa, CA 92626
(714) 957-3158
(ER) (FR) (RC) (VE)
CIRCLE 732

Palo Alto Design Group
360 University Ave.
Palo Alto, CA 94301
(415) 617-9623
(CM) (GP) (EP)
CIRCLE 733

Panduit Corp.
17301 S. Ridgeland Ave.
Tinley Park, IL 60477-0981
(800) 777-3300
(TB)
CIRCLE 734

Panel Controls Corp.
1000 Mt. Elliot
Detroit, MI 48207
(313) 568-2400
(RA) (VR)
CIRCLE 735

Parker Seal
Conductive Products
P.O. Box 11751
Lexington, KY, 40512
(800) 272-7537
(ER) (GK) (EL) (SA)
CIRCLE 736

Penstock Inc.
520 Mercury Dr.
Sunnyvale, CA 94086-4018
(408) 730-0300
(CM) (MP) (MI)
CIRCLE 737

Permagile Industries Inc.
Insulcast Div.
101 Commercial St.
Plainview, NY 11803
(516) 349-1100
(EL) (EN) (EA) (PM) (RE)
CIRCLE 738

Philips Components
Discrete Products Div.
2001 W. Blue Heron Blvd.
Riviera Beach, FL 33404
(407) 881-3208
(CE) (MM)
CIRCLE 739

Phoenix Mecano Inc.
Bopla Enclosures
7330 Executive Way
Frederick, MD 21701
(301) 696-9300
(BM) (CN) (EM) (IN) (PT) (RA) (ER) (GK)
CIRCLE 740

Plaskon Electronic Materials
A Rohm & Haas Co.
Independence Mall West
Philadelphia, PA 19105
(215) 592-2095
(EN)
CIRCLE 741

Pneumafil Corp.
Metal Products Div.
4500 Chesapeake Dr.
Charlotte, NC 28297
(704) 399-7441
(CN) (CM) (EM) (GP) (MI) (RA) (VR) (WT) (ES) (ER) (GK)
CIRCLE 742

Powerbox Inc.
1720 14th St.
Boulder, CO 80302
(303) 444-1461
(IN)
CIRCLE 743

Premier Metal Products Co.
381 Canal Pl.
Bronx, NY 10451
(718) 993-9200
(BM) (CN) (CM) (EN) (GP) (IN) (PT) (RA) (VR)
CIRCLE 744

Pulizzi Engineering Inc.
3260 S. Susan St.
Santa Ana, CA 92704-6865
(714) 540-4229
(BM) (CM) (EM) (GP) (MI) (PT) (RA) (VR) (ER)
CIRCLE 745

Quadrant Technology Inc.
999-C Edgewater Blvd. #277
Foster City, CA 94404
(415) 349-3095
(MP)
CIRCLE 746

Qualitek International Inc.
315 Fairbank St.
Addison, IL 60101
(708) 628-8083
(EA) (FL) (SO)
CIRCLE 747

Quantum Materials Inc.
9938 Via Pasar
San Diego, CA 92126
(619) 695-1716
(EA) (IK) (TF)
CIRCLE 748

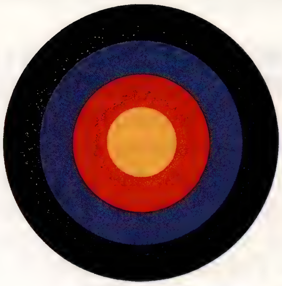
Quartzite Processing Inc.
6 Holyoke St.
Malden, MA 02148
(617) 322-3611
(CE)
CIRCLE 749

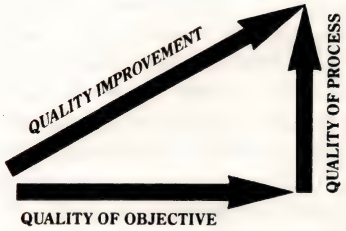
R.H. Carlson Co. Inc.
Norlabs Div.
41 Chestnut St.
Greenwich, CT 06830
(203) 531-5500
(CC) (EN) (EA) (PM) (RE)
CIRCLE 750

RTP Co.
580 E. Front St.
Winona, MN 55987-0439
(800) 433-4787
(EP)
CIRCLE 751

Radstone Technology Corp.
20 Craig Rd.
Montvale, NJ 07645
(201) 393-2700
(CM) (EM) (MI) (RA) (WT)
CIRCLE 752

(see p. 146 for key)
(continued on p. 142)





In fact, we're the first domestic capacitor maker to earn ISO 9001 registration. We did it by continually keeping your needs in our sights.

Our Company-Wide Quality Concept includes continual monitoring of your satisfaction with our present products and services.

To create new products to meet your needs, we utilize the KEMET Advanced Quality Planning System. It's thoroughly based on the performance levels and operating specs you establish for your new products—and it drives our design, development, and manufacture of new KEMET products.

To score big against your competition, team-up with a trading partner that stays in front by putting you first. KEMET.

We Help You Hit Your Targets.

KEMET®
Electronics Corporation

P.O. Box 5928 Greenville, SC 29606
803/963-6348

U.S.A., Newport Beach, CA, Phone: (714) 640-9320, FAX: (714) 720-9807; **Irving, TX,** Phone: (214) 556-0009, FAX: (214) 401-0254; **Schaumburg, IL,** Phone: (708) 517-1030, FAX: (708) 517-1037; **Wakefield, MA,** Phone: (617) 245-4646, FAX: (617) 245-1595; **Greenville, SC,** Phone: (803) 242-5789, FAX: (803) 242-5795; **EUROPE, Switzerland,** Phone: 41-22-738-4244, FAX: 41-22-738-3918; **Germany,** Phone: 49-89-46-30-01, FAX: 49-89-46-04-117; **France,** Phone: 33-1-46-87-70-95, FAX: 33-1-49-78-06-63; **United Kingdom,** Phone: 44-279-757-343, FAX: 44-279-757-188; **ASIA, Hong Kong,** Phone: 852-770-5633, FAX: 852-770-5656; **Singapore,** Phone: 65-227-2225, FAX: 65-227-2224; **Taiwan ROC,** Phone: 886-2-752-8585, FAX: 886-2-721-3129; **Korea,** Phone: 82-02-599-7131, FAX: 82-02-533-8089

CIRCLE 273 FOR U.S. RESPONSE

CIRCLE 274 FOR RESPONSE OUTSIDE THE U.S.

▼ LOW-FORCE EMI GASKETS TERMINATE THEMSELVES

Specifically designed for commercial electronic enclosures and metallized plastic housings, the Soft-Shield II EMI gaskets are self-terminating devices that require low closure forces. The gaskets provide 60-dB attenuation from 30 MHz to 1 GHz. Less than 1 lb./in force is required for the gaskets' foam core to seal an opening. This enables enclosures to be designed with fewer fasteners and thinner panels. Seven standard cross sections are offered as are custom shapes. Call for pricing and delivery information.

Chomerics Inc.
77 Dragon Ct.
Woburn, MA 01888
(617) 935-4850
▶CIRCLE 835

▼ PIN FIN HEAT SINKS COOL INTEL'S PENTIUM

A family of direct-mount pin fin heat sinks is designed for use with Intel's Pentium processor, 21-by-21-mm PGAs, and other high-performance ICs requiring enhanced heat dissipation. Maximum heat transfer of up to 18 W is possible in applications with limited air flow and space. The 698 Series heat sinks yield forced convection sink-to-ambient thermal-resistance values of 1.4°C/W at 100 lfm and 0.75°C/W at 400 lfm. Delivery of four standard models is from stock. Call for pricing.

EG&G Wakefield Engineering Inc.
60 Audubon Rd.
Wakefield, MA 01880
(617) 245-5900
▶CIRCLE 836

▼ PANELS SHIELD PCB-MOUNT CONNECTORS

Shielding of pc-board-mounted I/O connectors is performed by a line of panels constructed of urethane foam bonded within metallized fabric. The panels supply millions of electrical contact points and an excellent mechanical fit. Cutouts in the panels match connector cutouts and sizes. The panels, which are mounted between the backfence and chassis, attach to the backfence by means of an aggressive pressure-sensitive adhesive. Under minimal compression, the panels close gaps around the perimeter of the connector shell.

Schlegel Corp.
P.O. Box 23197
Rochester, NY 14692-3197
(800) 828-6237
▶CIRCLE 837

PACKAGING AND MATERIALS MANUFACTURERS

Ray Products Co. Inc.
11565 Federal Dr.
El Monte, CA 91731
(818) 579-4250
(CM) (IN) (PT) (ER)
CIRCLE 753

Resdel Corp.
Cape May County Ind. Park
Rio Grande, NJ 08242
(609) 886-1111
(EM) (GP) (TB)
CIRCLE 754

Revere Aerospace Inc.
845 N. Colony Rd.
Wallingford, CT 06492
(203) 269-7701
(ER)
CIRCLE 755

Ribbon Cable Co.
8753 Lion St.
Rancho Cucamonga, CA 91730
(714) 987-0007
(ER)
CIRCLE 756

Richmond Technology Inc.
1897 Colton Ave.
Redlands, CA 92374
(909) 794-2111
(ES) (ER)
CIRCLE 757

Rittal Corp.
One Rittal Pl.
Springfield, OH 45504
(513) 399-0500
(CN) (EM) (GP) (IN) (MP) (PT) (RA) (VR) (WT)
CIRCLE 758

Robison Electronics Inc.
3580 Sacramento Dr.
San Luis Obispo, CA 93403-8121
(805) 544-8000
(PM)
CIRCLE 759

Rogers Corp.
Composite Materials Div.
One Technology Dr.
Rogers, CT 06263
(203) 774-9605
(LA)
CIRCLE 760

Rogers Corp.
Microwave & Circuit Materials
100 S. Roosevelt Ave.
Chandler, AZ 85226
(602) 961-1382
(LA)
CIRCLE 761

Rogers Corp.
Molding Materials Div.
P.O. Box 550
Manchester, CT 06040
(203) 646-5500
(EP)
CIRCLE 762

Rogers Corp.
Poron Materials Div.
P.O. Box 158
E. Woodstock, CT 06244
(203) 774-9605
(GK) (SE)
CIRCLE 763

SIMCO
P.O. Box 1009
Miami, FL 33197
(305) 233-9900
(GP) (IN) (PT) (ER) (EP)
CIRCLE 764

SMI Ceramics America Inc.
2953 Bunker Hill Ln. #203
Santa Clara, CA 95054
(408) 982-0990
(MP) (ER) (CE)
CIRCLE 765

Santa Fe Textiles Inc.
16951 Murphy Ave.
Irvine, CA 92714
(714) 251-1960
(ER) (TB)
CIRCLE 766

Sauereisen Cements
160 Gamma Dr.
Pittsburgh, PA 15238
(412) 963-0303
(EN) (EA) (PM)
CIRCLE 767

Schaffner EMC Inc.
9 Fadem Rd.
Springfield, NJ 07081
(201) 379-7778
(ER)
CIRCLE 768

Schlegel Corp.
Industrial Products Div.
P.O. Box 23197
Rochester, NY 14692-3197
(800) 828-6237
(ES) (ER) (GK)
CIRCLE 769

Schroff Inc.
170 Commerce Dr.
Warwick, RI 02886
(401) 732-3770
(BM) (CN) (EM) (GP) (IN) (PT) (RA) (VR)
CIRCLE 770

Sescom Inc.
2100 Ward Dr.
Henderson, NV 89015-4249
(702) 565-3400
(BM) (GP)
CIRCLE 771

Shin-Etsu Polymer America Inc.
34135 7th St.
Union City, CA 94587
(510) 475-9000
(EL) (IK) (MM)
CIRCLE 772

Shogyo International Corp.
287 Northern Blvd.
Great Neck, NY 11021
(516) 466-0911
(BM) (CN) (CM) (GP) (IN) (PT) (ES) (FR) (MG) (EL) (EP) (EA) (LA)
CIRCLE 773

Specialty Coating Systems Inc.
5707 W. Minnesota St.
Indianapolis, IN 46241
(317) 244-1200
(CC)
CIRCLE 774

Spira Mfg. Corp.
12721 Saticoy St. South
North Hollywood, CA 91605
(818) 764-8222
(ER) (GK)
CIRCLE 775

Stevens Products Inc.
128 N. Park St.
East Orange, NJ 07019
(201) 672-2140
(CM) (MI) (ER) (TB) (EP) (LA) (PM)
CIRCLE 776

Strongbox
P.O. Box 2726
Culver City, CA 90231-2726
(310) 305-8288
(CM) (GP) (MI) (RA)
CIRCLE 777

Sumitomo Metal Mining USA Inc.
Boston Office
12 Alfred St., Suite 300
Woburn, MA 01801
(617) 932-6208
(CE) (MM) (TF)
CIRCLE 778

TRA-CON Inc.
55 North St.
Medford, MA 02155
(617) 391-5550
(ES) (ER) (GK) (CE) (CC) (EN) (EP) (EA) (IK) (PM) (RE)
CIRCLE 779

Taiyo America Inc.
1179 Fairview Dr., Suite E
Carson City, NV 89701
(702) 885-9959
(IK) (SM)
CIRCLE 780

Techform Laboratories Inc.
2021 N. Glassell St.
Orange, CA 92665
(714) 921-9054
(CC) (EN) (EA) (PM)
CIRCLE 781

Techmar Corp.
5420 McConnell Ave.
Los Angeles, CA 90066
(800) 832-4627
(IN)
CIRCLE 782

Technit Inc.
129 Dermody St.
Cranford, NJ 07016
(908) 272-5500
(ER) (GK) (VE) (WN)
CIRCLE 783

Temp-Flex Cable Inc.
11 Depot St.
South Grafton, MA 01560
(508) 839-5987
(ER)
CIRCLE 784

The Carborundum Co.
Microelectronics Div.
10409 S. 50th Pl.
Phoenix, AZ 85044
(602) 496-5000
(CE) (SU)
CIRCLE 785

(see p. 146 for key)
(continued on p. 144)

We're not just number one in the world... we're number ISO 9002!

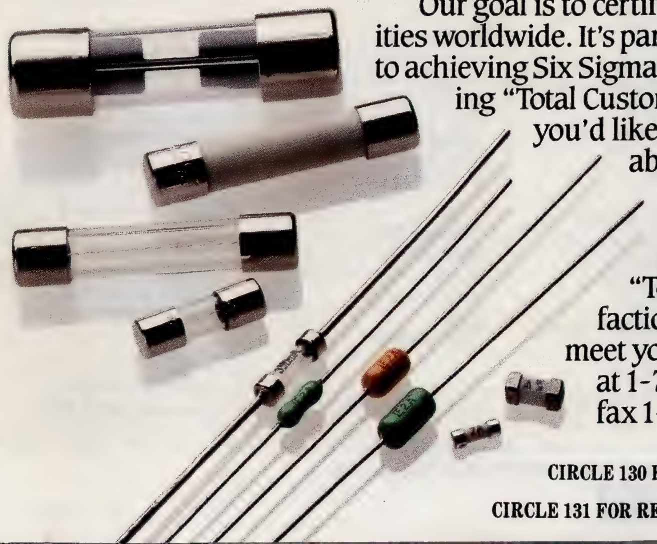
In today's global marketplace your suppliers have to be more than number one. They have to have an ISO 9000 number, too!

That's why at Littelfuse we give you both.

Our most recent certification of our Centralia, Illinois facility to ISO 9002 by INTERTEK is our second U.S. facility and our fourth facility worldwide to have earned ISO 9000 registration. No other U.S. circuit protection fuse manufacturer can claim to have certified even one of its domestic facilities.

To our customers, the ISO 9002 certification of our small dimension and surface mount fuse manufacturing facilities in Centralia, Illinois and in Washington, England serve as independent confirmation that Littelfuse is better able to meet your quality systems expectations.

Our goal is to certify all Littelfuse facilities worldwide. It's part of our commitment to achieving Six Sigma quality and providing "Total Customer Satisfaction." If you'd like more information about how Littelfuse ISO registration, Six Sigma quality objectives and "Total Customer Satisfaction" programs can meet your needs, call us at 1-708-824-0400 or fax 1-708-824-3024.



Littelfuse®

Littelfuse Inc.

CIRCLE 130 FOR U.S. RESPONSE

CIRCLE 131 FOR RESPONSE OUTSIDE THE U.S.

POWER SOURCES

▼ 3-BY-5-IN. SWITCHER HITS 120-W PEAK

Modifications and semi-custom derivatives are available for a family of 3-by-5-in. universal-input ac-dc switchers. Units are available from 50 to 120 W as well as in 150-, 250-, and 350-W product families. Semi-custom and modified units don't compromise existing safety-agency approvals. The company's Easymod service enables as few as 100 units per year to be modified to specific user needs. Normal turnaround for prototypes is less than four weeks with production lead time at six weeks after approval. Call for pricing.

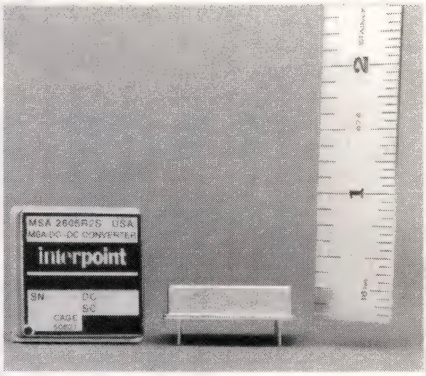
Power Solutions Inc.
Easymod Applications
4699 N. Federal Hwy.
Pompano Beach, FL 33064
(516) 627-5628
▶ CIRCLE 838

▼ MONOLITHIC DRIVERS SUIT MOTOR CONTROL

Claimed as the industry's only monolithic driver ICs rated for 80-V, n-channel power-MOSFET H bridges, the HIP4080 (input comparator) and HIP4081 (four independent inputs) driver ICs suit motor controls, power supplies, audio amplifiers, and uninterruptible power supplies. The ICs offer twice the operating voltage, five times the drive capability, and 10 times the PWM frequency of its nearest competitor. The units handle 80 V at 2.5 A while switching into a 1000-pF load at 1 MHz with typical rise and fall times of 10 ns. This translates into lower switching losses and permits use of smaller, less costly filter components. In lots of 1000, the HIP4080 and HIP4081 cost \$3.50 in 20-lead plastic DIPs and \$3.71 in 20-lead SOICs. Delivery is from stock.

Harris Semiconductor
P.O. Box 883
Melbourne, FL 32901
(800) 4-HARRIS
▶ CIRCLE 839

▼ LOW-PROFILE CONVERTER TAKES 80-V SURGES



A low-profile, 5-W dc-dc converter with a 5.2-V output offers an input-voltage surge rating of 80 V. The MSA 285R2S converter's output enables designers to drive ECL components at optimal speed, or to accommodate voltage drops to the load, without adding any external components. The high input-voltage transient rating (to 80 V for 50 ms) meets MIL-STD-704 requirements and eliminates the need for separate input-protection circuitry. Input voltage is rated for 16 to 40 V dc with line and load regulation typically rated at 10 mV. The converter's low 0.265-in. height enables designers to use minimal board-to-board spacing and to reduce overall system size. Pricing in lots of 100 is \$243 with delivery from stock to six weeks.

Interpoint Corp.
P.O. Box 97005
Redmond, WA 98073-9705
(206) 882-3100
▶ CIRCLE 840

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Thermagon Inc.
3256 W. 25th St.
Cleveland, OH 44109-1668
(216) 741-7659
(EL) (EN) (EA) (SU)
CIRCLE 786

Trans Tech America Inc.
655 W. Wise Rd.
Schaumburg, IL 60193
(708) 893-7521
(IK)
CIRCLE 787

Transene Co. Inc.
Rte. 1 Tpke.
Rowley, MA 01969
(508) 948-2501
(CC) (EL) (EN) (EA) (PC) (PM)
CIRCLE 788

UVEXS Inc.
580 N. Pastoria Ave.
Sunnyvale, CA 94086
(408) 737-7100
(EN) (EA) (IK)
CIRCLE 789

Underwater Kinetics
1020 Linda Vista Dr.
San Marcos, CA 92069
(619) 744-7560
(CM) (EM) (GP) (IN) (MI) (PT) (WT) (ES) (ER) (GK) (VE) (EL) (EP) (RE)
CIRCLE 790

Uniroyal Technology Corp.
Uniroyal Adhesives & Sealants
312 N. Hill St.
Mishawaka, IN 46544
(219) 256-8655
(EA)
CIRCLE 791

Uniroyal Technology Corp.
Ensolite Div.
312 N. Hill St.
Mishawaka, IN 46544
(219) 256-8177
(GK)
CIRCLE 792

Urban Chemical Co. Inc.
151 S. Pfingsten Rd.
Deerfield, IL 60015
(708) 498-3080
(CC) (FL) (SO)
CIRCLE 793

Vector Electronic Co.
12460 Gladstone Ave.
Sylmar, CA 91342
(800) 426-5659
(BM) (CM) (EM) (GP) (IN) (RA)
CIRCLE 794

Vemaline Products
333 Strawberry Field Rd.
Warwick, RI 02887-6979
(401) 739-7600
(HS)
CIRCLE 795

Videojet Systems Int'l. Inc.
1500 Mittel Blvd.
Wood Dale, IL 60191
(800) 654-4663
(IK)
CIRCLE 796

Vista Performance Polymers
900 Threadneedle
Houston, TX 77079
(713) 588-3515
(EP)
CIRCLE 797

Vynckier Inc.
Hwy. 22 North, P.O. Box 910
Mankato, MN 56002-0910
(507) 345-2572
(BM) (GP) (IN) (PT) (AR) (WT)
CIRCLE 798

W. L. Gore & Assoc.
Electronic Products Div.
555 Papermill Rd.
Newark, DE 19711
(302) 738-4880
(ER) (GK) (SE) (VE) (LA) (SU) (TF)
CIRCLE 799

W. L. Gore & Associates Inc.
Electronic Products Div.
4755 E. Beautiful Ln.
Phoenix, AZ 85044
(602) 431-0077
(ER) (GK) (RC) (LA)
CIRCLE 800

W. L. Gore & Associates Inc.
Electronics Products Div.
2401 Singerly Rd.
P.O. Box 1220
Elkton, MD 21922
(410) 398-6400
(ER) (GK) (SE) (VE)
CIRCLE 801

Wamco Inc.
W. A. Miller Co. Inc.
Mingo Loop, P.O. Box 337
Oquossoc, ME 04964-0337
(800) 227-1415
(BM) (CM) (GP) (IN) (PT) (RA) (WT)
CIRCLE 802

Wieland Inc.
466 Main St.
New Rochelle, NY 10801
(914) 633-0222
(RA)
CIRCLE 803

Wilson Case Inc.
Industrial Park East, Bldg. 37
P.O. Box 1106
Hastings, NE 68902-1106
(800) 322-5493
(CM) (IN) (MI) (PT) (WT)
CIRCLE 804

Woodbine Industries Inc.
1574 Bridgewater Rd.
Bensalem, PA 19020
(215) 638-7600
(BM) (CN) (CM) (EM) (GP) (MI) (PT) (RA) (VR) (WT) (ER)
CIRCLE 805

Z Systems Inc.
3080 Olcott St., #110 C
Santa Clara, CA 95054
(408) 980-1563
(MP) (SU)
CIRCLE 806

Zero Stantron Cabinets
12224 Montague St.
Pacoima, CA 91331-2226
(818) 890-3445
(BM) (CN) (CM) (EM) (GP) (IN) (RA) (VH) (WT)
CIRCLE 807

(see p. 146 for key)
(continued on p. 146)

PCMCIA THE SMART WAY

Here's why SMART Modular Technologies is the smart way to get PCMCIA cards. *Innovation:* Our SmartRAM technology puts Flash memory and SRAM onto one incredibly versatile card. Our unique PSRAM with Battery Back-up cards protect valuable data. *Low power consumption:* Our custom ASICs are geniuses at power management. Our Fax/Modem cards have an ultra low power sleep mode. *Quality:* SMART has ISO 9001 certification in process. *Reliability:* Rugged mechanical design. Fortune 500 Qualified manufacturing. *Versatility:* We have whole families of all the card types you see here. JEIDA/JEDEC DRAM cards, too And we'll handle custom cards from start to finish. SMART. The company to call for PCMCIA.

14.4K baud Fax/Modem cards

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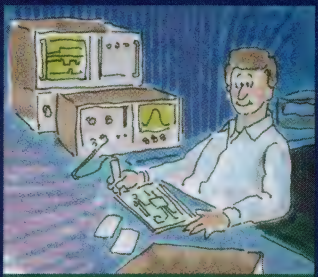
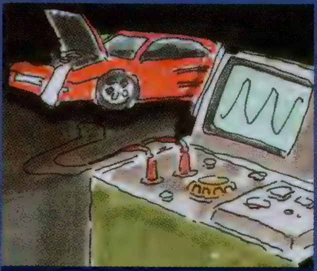
Data logger: Flash memory cards


Instrumentation: SRAM cards


Auto diagnostics: OTP ROM cards

PDAs: PSRAM cards

Patient cards: SmartRAM cards

Your custom card

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SMART
Modular Technologies

45531 Northport Loop West, Fremont, CA 94538
Tel: 510.623.1231, Fax: 510.623.1434
1.800.536.1231

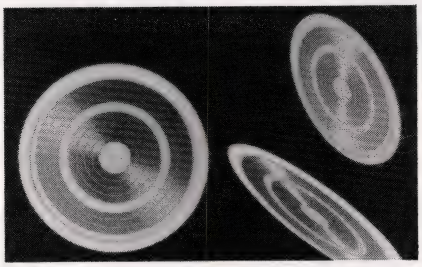
CIRCLE 279 FOR U.S. RESPONSE CIRCLE 280 FOR RESPONSE OUTSIDE THE U.S.

▼ THIN BATTERIES DRIVE APPLE'S POWERBOOK

The ThinLine batteries from Portable Energy Products Inc. are at the heart of Technöggin Inc.'s PowerPlate rechargeable power systems for Apple's PowerBook laptop computers. The systems are thin, lightweight battery packs that offer up to five times the life of the PowerBooks' internal batteries alone. The ThinLine energy cells use sealed lead chemistry and provide from 40 to 60% higher energy density than earlier batteries made with the same technology. Call for pricing and delivery information.

Portable Energy Products Inc.
940 Disc Dr.
Scotts Valley, CA 95066
(408) 439-5100
▶ **CIRCLE 841**

▼ GTO THYRISTORS NEED SMALLER SNUBBERS



A de-alloy process technique used in the fabrication of the FG2000EX-50D (2500 V/2000 A) and FG4000CX-90D (4500 V/4000 A) GTO thyristors enables the use of smaller snubber capacitors for lower system cost and improved thermal capacities. Finer cathode patterns also contribute to the shift to smaller capacitors. The GTO devices are designed for use in inverters for application on rapid-transit systems and utility power apparatus as wel as large industrial ac-motor controls. Typical pricing in lots of 10 is $1383 for the 2500-V devices and $4300 for the 4500-V types. Prototype quantities are delivered in four to six weeks.

Powerex
Hillis St.
Youngwood, PA 15697
(412) 925-4488
▶ **CIRCLE 842**

▼ TINY 1-W CONVERTERS TAKE MINIMAL SPACE

Reliable performance is coupled with minimum space consumption in the 100FS Series of ultra-miniature 1-W dc-dc converters. The single-in-line packaged devices take just 0.18 in.^{2} of board space. Eleven models operate from 5 or 12 V dc and provide single and dual outputs of 5, 9, 12, 15, ±5, ±12, or ±15 V dc. All offer 500-V dc I/O isolation, high efficiency, and low-noise operation. In lots of 100, pricing starts at $8.40. Delivery is from stock to four weeks.

Conversion Devices Inc.
15 Jonathan Dr.
Brockton, MA 02401
(508) 559-0880
▶ **CIRCLE 843**

▼ 500-W CASED SWITCHERS HAVE WIDE OUTPUTS

A compact, low-profile case size of 2.45 by 5.0 by 9.4 in. with output power of up to 500 W is offered by the Uniflex XN series of switchers. The supplies have a 5-V main output at 60 or 70 A and up to three auxiliary outputs that are adjustable over wide voltage ranges. The auxiliary outputs are quickly configured to user requirements from three standard modules: 2 to 6 V dc at 90 W; 5 to 15 V dc at 150 W, and 15 to 36 V dc at 150 W. From these modules, any combination of output voltages can be configured from 2 to 36 V dc. All outputs are independent and isolated. Power density is 4.3 W/in.^{3} with internal cooling by a 60-mm dc ball-bearing fan. Unit prices start at $455 with OEM quantities at $319. Samples are available in two weeks with production lots delivered in eight weeks from receipt of order.

Unipower Corp.
2981 Gateway Dr.
Pompano Beach, FL 33069
(305) 974-2442
▶ **CIRCLE 844**

▼ STEP-UP CONVERTERS POWER PORTABLES

Delivering 250 mA of output current at 5 V from a 2-V supply, the LT1300 dc-dc converter has applications in palmtop computers, portable instruments, hand-held bar-code scanners, and other portable systems. The device provides up to 88% efficiency from supplies as low as 1.8 V. Quiescent current is 120 μA and the device can be shut down to 10 μA of standby current. It's programmable for 3.3-V or 5-V output by means of a logic-controlled input pin. The on-chip power switch has a saturation voltage of 170 mV at a switch current of 1 A, which represents a four-fold reduction from earlier dc-dc converters. Pricing for the 8-pin DIP version is $3 in lots of 100. An SOIC version costs $3.20. Samples are available now.

Linear Technology Corp.
1630 McCarthy Blvd.
Milpitas, CA 95035-7487
(800) 637-5545
▶ **CIRCLE 845**

PACKAGING AND MATERIALS MANUFACTURERS

Zero-East
Zen Plastics
288 Main St.
Monson, MA 01057-0128
(413) 267-5561
(CM) (EM) (GP) (MI) (RA)
CIRCLE 808

Zippertubing Co.
P.O. Box 61129
Los Angeles, CA 90061
(310) 527-0488
(EM) (MI) (ER) (MG) (SE)
(TB) (EN) (PM)
CIRCLE 809

Zoltech Corp.
16658 Arminta St.
Van Nuys, CA 91406
(818) 780-1800
(BM) (CM) (EM) (GP) (IN)
(RA) (VR) (ER)
CIRCLE 810

Zymet Inc.
7 Great Meadow Ln.
East Hanover, NJ 07936
(201) 428-5245
(EA)
CIRCLE 811

KEY

Enclosures and Packages

(BM)	Bench mounted
(CN)	Consoles
(CM)	Custom design
(EM)	EMI/RFI design
(GP)	General purpose
(HS)	Heat sinks
(IN)	Instrument cases
(MP)	Microcircuit packages
(MI)	Military design
(PT)	Portable
(RA)	Racks
(VR)	Vertical racks
(WT)	Water tight

Materials

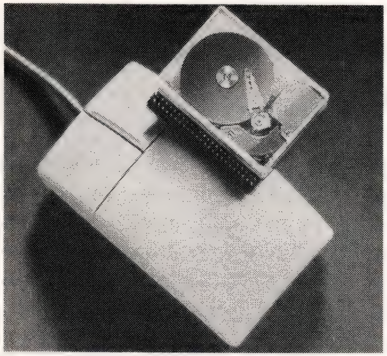
(CE)	Ceramics
(CC)	Conformal coatings
(EL)	Elastomers
(EN)	Encapsulants
(EP)	Engineering plastics
(EA)	Epoxies & adhesives
(PF)	Films, piezo
(FP)	Films, polyester
(FE)	Films, polyimide
(FL)	Fluxes
(IK)	Inks
(LA)	Laminates
(MM)	Magnetic materials
(MC)	Metal matrix composites
(MF)	Metalized fabrics
(PC)	Passivation coatings
(PM)	Potting materials
(RE)	Resins
(SA)	Seals
(SO)	Solders
(SM)	Solder masks
(SU)	Substrates
(TF)	Thick films

Shielding

(ES)	Electrostatic
(ER)	EMI/RFI
(FR)	Ferrites
(GK)	Gaskets
(MG)	Magnetic
(RC)	Rooms, chambers
(SE)	Sheets/strips
(TB)	Tubing
(VE)	Vents
(WN)	Windows

▼ CUSTOM CONNECTORS FIT HP'S KITTYHAWK

Custom connectors are now available for users of Hewlett Packard's Kittyhawk personal storage module.

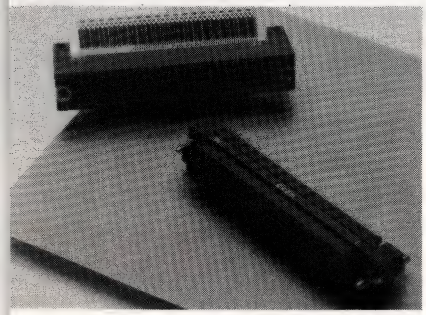


The connectors enable designers to efficiently mount either the 21.4- or 42.8-Mbyte versions of the 1.3-in. hard-disk drive directly on pc boards. Two connector solutions are offered. The IC6 Series is for the PCMCIA-connector models, while the HRUS-0170 Series is a 6-mm-high, 2-mm-pitch through-hole socket that enables the ATA version of the drive to be mounted in an inverted manner. Call for pricing and delivery.

Hirose Electric (U.S.A.) Inc.
2688 Westhills Ct.
Simi Valley, CA 93065
(805) 522-7958
▶ CIRCLE 902

▼ SEM-E CONNECTOR OFFERS LIGHT WEIGHT

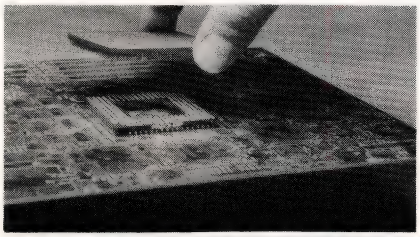
A lightweight, low-cost plastic SEM-E-style connector has joined a family of high-density printed-circuit connectors. Available in both through-hole-mount receptacle and surface-mount plug styles, the 152-contact devices cost about half as much as competing metal-shelled units. They suit high-reliability commercial signal-interconnect applications that require a high pin count in a very small area. Each of the 152 contacts offers a curent rating of 2.5 A with a contact resistance of less than 126 mΩ. The connectors are rated for a dielectric withstanding voltage of 600 V ac with insulation resistance of 5000 MΩ at 500 V dc. OEM pricing is less than $90 per mated pair. Prototype quantities are delivered in less than 30 days.



Packard-Hughes Interconnect
17150 Von Karman Ave.
Irvine, CA 92714
(800) 821-2998
▶ CIRCLE 903

▼ LOW-FORCE SOCKET ACCEPTS LARGE PGAs

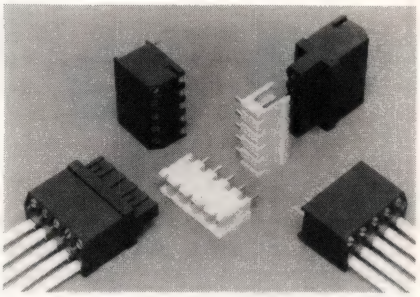
PGA devices with 200 or more pins can be inserted by hand into the Ultra Lite low-insertion-force sockets. Thanks to a fourth-generation contact specifically designed for the socket, demonstrated insertion forces are a low 0.58 ozs/pin while extraction forces are 0.39 ozs/pin. The socket is suited for use with high-pin-count devices such as RISC processors and multichip modules, which now carry some 400 pins and are expected to have well over a thousand in the next few years. Call for pricing and delivery.



Mill-Max Mfg. Corp.
190 Pine Hollow Rd.
Oyster Bay, NY 11771
(516) 922-6000
▶ CIRCLE 904

▼ TERMINAL BLOCKS STACK END-TO-END

A modular, interlocking terminal-block connector is available for applications in process- and traffic-control equipment; telecommunication equipment; and HVAC, fire-alarm, and security systems. The Termi-Blok connector comes in one-piece right-angle and vertical pcb-mount versions and two-piece plug versions with mating headers. Connectors are stackable end-to-end without loss of their 0.200-in. centerline spacing. Screw-clamp contacts accept 24 to 12 AWG solid or stranded wire with entry parallel to the screw. Pricing in lots of 5000 is $0.22 per line for the one-piece version and $0.37 per line for the two-piece version. Delivery is in one to four weeks.



AMP Inc.
P.O. Box 3608
Harrisburg, PA 17105-3608
(800) 522-6752
▶ CIRCLE 905

▼ DUAL-ROW SMT CONNECTOR MEETS MIL-C-83513 SPECS

A dual-row, surface-mount connector offers 0.050-in. centers and is based on the company's Flex Pin design. It features a one-piece stamped contact with an integral tail. Designed to meet MIL-C-83513 specifications, the connectors' rear is sealed with epoxy to protect the contact from solder wicking. Guide posts for alignment and/or keying are available. Male and female versions are offered with up to 97 contacts. In the 97-contact configuration, the connector is just 2.77 in. long including its mounting ears.

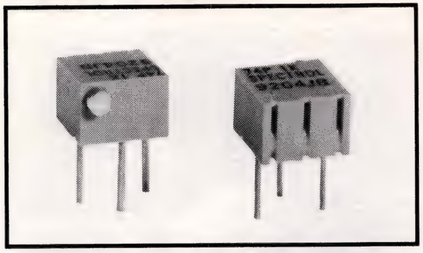
Omnetics Connector Corp.
7260 Commerce Circle East
Minneapolis, MN 55432-3103
(612) 572-0656
▶ CIRCLE 906

▼ VIDEO PATCH JACKS HAVE 720-MHZ BANDWIDTH

An extended bandwidth of dc to 720 MHz is now offered by a line of 75-Ω video patch jacks. With the addition of the J24WHF, a high-frequency version of the J14 Series of normal-through patch jacks (BNC rear interface), the line is suited for serial digital applications. Also offered is the self-terminating model J24WTHF-75 dual coax patch jack. Typical return loss for the connectors is greater than 40 dB through 720 MHz. Call for pricing and delivery information.

Trompeter Electronics Inc.
P.O. Box 5069
Westlake Village, CA 91362-4047
(818) 707-2020
▶ CIRCLE 907

12 Turn Trimmer From Spectrol is Only 1/4″ Square

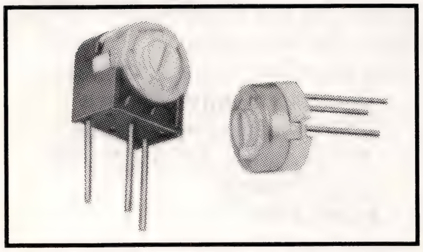


Save space and money with the compact, economical Model 74 from Spectrol. The cermet element assures excellent setting stability over a resistance range of standard values from 10 ohms through 1 megohm. Resistance tolerance is rated ±10%. Model 74 is available in 3 pin styles for top or side adjustment and also features solder plated terminals, a Tempco of ±100 ppm/°C, and a CRV of 3% or 3 ohms. The case is sealed to withstand 85°C for one minute during solvent or aqueous cleaning. Manufactured to meet the highest reliability standards, the Model 74 is environmentally and performance tested to MIL-STD-202 and MIL-R-22097.

Spectrol®

Spectrol Electronics Corporation
4051 Greystone Drive, Ontario, CA 91761
Phone: (714) 923-3313 Fax: (714) 923-6765
CIRCLE 181 FOR U.S. RESPONSE
CIRCLE 182 FOR RESPONSE OUTSIDE THE U.S.

1/4″ Round Single-Turn Trimmer Meets MIL Spec



Spectrol's new 1/4″ round single-turn cermet trimmer, the Model 75, offers three package/terminal styles to choose from. The unit is available in side-adjust or two different top-adjust versions, with pin configurations to suit standard PCB applications. This low-cost space-saver is available in resistance ranges from 10 ohms to 2 megohms with a ±10% resistance tolerance. It features soldered terminations, integral multifinger wiper, superior setability and stability, a TEMPCO of ±100 PPM/°C, a CRV of 3%, and is sealed for solvent and aqueous cleaning. Tested to MIL-R-22097.

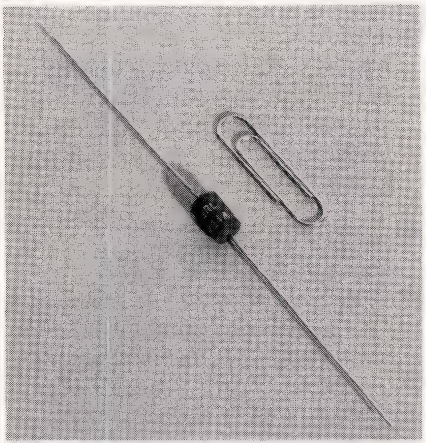
Spectrol®

Spectrol Electronics Corporation
4051 Greystone Drive, Ontario, CA 91761
Phone: (714) 923-3313 Fax: (714) 923-6765
CIRCLE 205 FOR U.S. RESPONSE
CIRCLE 206 FOR RESPONSE OUTSIDE THE U.S.

PASSIVE COMPONENTS

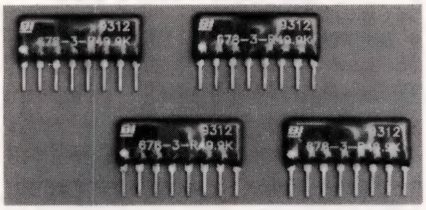
▼ WIREWOUND RESISTORS ARE COMPACT, PRECISE

Standard accuracy of 0.01%, a standard temperature coefficient of 5 ppm/°C, stability of better than 0.003%/year, and compact size are featured in the R-21A miniature encapsulated wirewound resistors. Measuring only 1/4 in. in diameter and 3/8 in. long, the resistor is well suited for applications requiring high stability and precision as well as small size. Standard resistance values range from 100 Ω to 150 kΩ. Standard accuracy is ±0.01% for values of 1 kΩ and higher, and ±0.05% or ±0.1% for values lower than 1 kΩ. Call for pricing and delivery.



Julie Research Laboratories Inc.
508 W. 26th St.
New York, NY 10001
(212) 633-6625
▶CIRCLE 908

▼ THIN-FILM NETWORKS WON'T WASTE SPACE



A series of precision, thin-film SIP resistor networks is offered as a complement to the company's DIP and SMT precision-network lines. The 670 Series combines the electrical performance of precision thin film with the space savings of a single in-line package. All networks in the series exhibit an excellent tracking-temperature coefficient of ±2 ppm/°C and ratio matches to ±0.02%. Standard circuits include both isolated and center-tapped configurations. Pricing starts at under $1.50 in lots of 1000. Delivery is from stock to eight weeks.

Beckman Industrial Corp.
4200 Bonita Pl.
Fullerton, CA 92631
(714) 447-2345
▶CIRCLE 909

▼ SNAP-MOUNT CAPACITORS SUIT POWER SUPPLIES

To meet the demand for autoranging input voltages and power-factor correction in switching power supplies, both of which require input-bus voltages of near 400 V dc, Cornell Dubilier has expanded its line of high-value, snap-mount aluminum capacitors. Types 380L/LX and 381L/LX offer ratings of 450 V dc at 105°C, case sizes from 20 mm in height and 20 mm in diameter, and ripple-current ratings to 10 A. Capacitance-voltage combinations range from 470 μF and 450 V dc through 68,000 μF and 16 V dc. Pricing ranges from $0.75 to $5 each in lots of 1000. Delivery is from stock to 12 weeks.

Cornell Dubilier
P.O. Box 128
Pickens, SC 29671
(803) 878-6311
▶CIRCLE 910

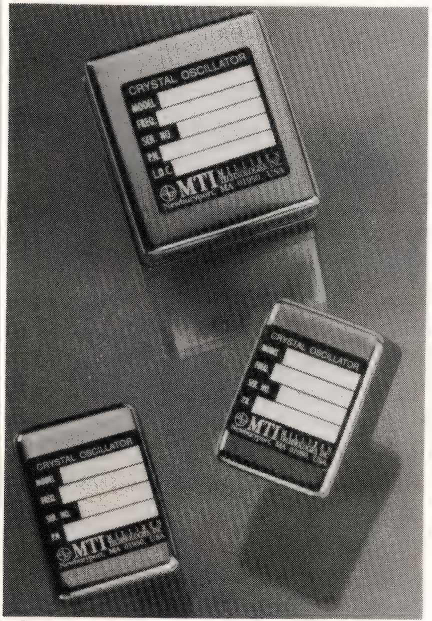
▼ DOUBLE-LAYER CAPS BACK UP MEMORIES

A range of double-layer capacitors is designed for power backup in semiconductor systems for devices such as CMOS memories. The DLC 196 capacitors are a reliable, cost-effective alternative to rechargeable batteries. They offer a very high charge-storage capacity per unit volume of about 2 C/cm^3. Standard versions range from 0.047 to 1 F with a rated voltage of 5.5 V and operating-temperature range of –25 to +70°C. Write for pricing and delivery.

Philips Components
Building BAE-1
P.O. Box 218
5600 MD Eindhoven
The Netherlands
▶CIRCLE 911

▼ CRYSTAL OSCILLATORS SUIT WORLDWIDE USES

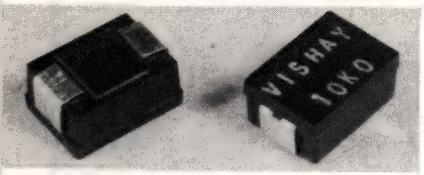
Three models form the International Series of crystal oscillators. The devices offer form, fit, and function replacement in many applications worldwide. Two models offer such high-performance features as ultra-low phase noise and high stability. A low-profile version features a maximum height of 13 mm. Standard frequencies are delivered from stock and pricing ranges from $145 to $365 in quantities of 100.



Milliren Technologies Inc.
Two New Pasture Rd.
Newburyport, MA 01950
(508) 465-6064
▶ CIRCLE 912

▼ SMT CHIP RESISTOR OFFERS HIGH PRECISION

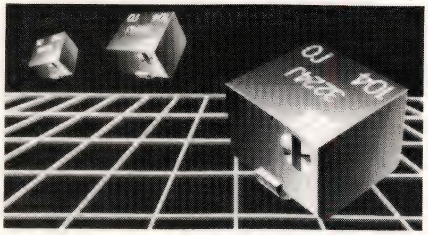
Excellent long-term stability of 0.005% for 2000 hours is offered by the SMR3 molded precision surface-mounted resistor. The devices' performance is similar to that of the company's S102 through-hole products. Use of a Bulk Metal foil resistive element results in a very low temperature coefficient of resistance and high stability. Values range from 5 Ω to 80 kΩ. Tolerance is specified at 0.01%. Welded internal leads result in a device that withstands significant thermal cycling. Call for pricing and delivery.



Vishay Resistors
63 Lincoln Hwy.
Malvern, PA 19355
(215) 644-1300
▶ CIRCLE 913

▼ SURFACE-MOUNT TRIMMER SAVES BOARD SPACE

The search for a miniature, multiturn trimming potentiometer may end with the Model 3224 4-mm device. The unit measures just 16 mm^2 as compared with 36 mm^2 for competing products, saving 50% more board space. The sealed component withstands IR-reflow or vapor-phase processes and is also available for through-the-wave soldering processes. The 11-turn device has a rotational life of 200 cycles. A broad range of values is offered from 10 Ω to 2 MΩ. Pricing is $1.98 in lots of 1000. Delivery is from stock to eight weeks.



Bourns Inc.
1200 Columbia Ave.
Riverside, CA 92507
(909) 781-5140
▶ CIRCLE 914

▼ SMT CHIP CAPACITORS SLASH LEAD TIMES

Reduced lead times are now offered for a complete line of surface-mounted chip capacitors. Delivery is now from stock to a maximum of three weeks. The extremely thin ceramic capacitors (0.5 mm maximum) can be mounted underneath PLCCs and SOJs used with SIMMs. They can also be used on multichip modules and come in four EIA sizes.

Circuit Components Inc.
2400 S. Roosevelt St.
Tempe, AZ 85282
(602) 967-0624
▶ CIRCLE 915

NEW!

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NEWEST FAMILY OF EXTERNAL SWITCHERS.

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MODEL	MAX. WATTS	OUTPUT VDC	OUTPUT AMPS	RIPPLE mV P-P	REGULATION
SW108KA0012F01	25	+5	0-5.0	50	±1%
SW109KA0012F01	25	+9	0-2.78	50	±1%
SW110KA0012F01	25	+12	0-2.08	50	±1%
SW111KA0012F01	25	+15	0-1.67	50	±1%
SW112KA0012F01	25	+16	0-1.56	50	±1%
SW113KA0012F01	25	+24	0-1.05	50	±1%
SW201KA0012F01	25	+5, +12	0-4.0, 0-1.0	50, 100	±1%, ±5%
SW301KA0012F01	25	+5, +12, –12	0-4.0, 0-1.0, 0-.6	5, 100, 100	±1%, ±5%, ±6%

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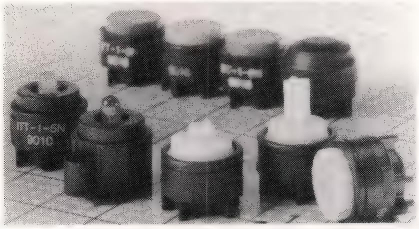
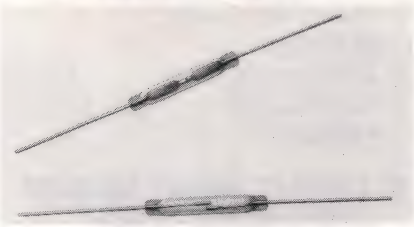
▼ SINGLE-POLE KEYSWITCH MEETS DEMANDING USES

A versatile, high-performance keyswitch is designed to meet the most demanding requirements. The K12 Series devices are wave-solderable, single-pole switches with gold contacts. Features include momentary, push-push, two make-point contacts; optional tactile feedback and operating force; variable travel; optional LED illumination and keycaps; and an available washdown version. Pricing ranges from $1.10 to $6.56 depending on quantity and style.



ITT Schadow Inc.
8081 Wallace Rd.
Eden Prairie, MN 55344
(612) 934-4400
▶CIRCLE 916

▼ 50-W POWER SWITCH HAS 750-V BREAKDOWN

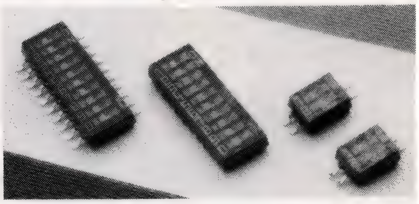


A miniature, SPST, normally open magnetic reed switch is designed for applications where high breakdown voltage is combined with power-load switching. The MRPR-8 switch has contacts rated at 50 W with a minimum breakdown voltage of 750 V dc. That breakdown voltage is midway between available switches with 250- and 1000-V dc ratings. Switch operation is facilitated by either a coil or a permanent magnet. Delivery is from stock to four weeks. Call for pricing.

Hamlin Inc.
612 E. Lake St.
Lake Mills, WI 53551
(414) 648-3000
▶CIRCLE 917

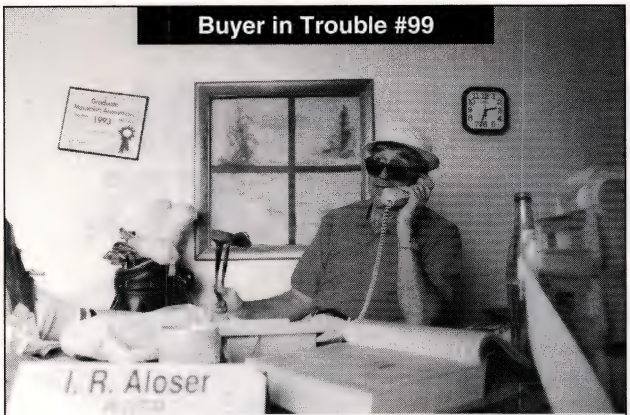
▼ SMT DIP SWITCHES MAKE MOST OF PCB SPACE

Available in 2, 4, 6, 8, and 10 positions and in standard small-outline packages, the CHS Series of surface-mounted DIP switches maximize use of board space, reduce end-product size, increase yields, and lower overall costs. The recently added 2- and 10-position versions (CHS02 and CHS10, respectively) feature a 0.050-in. lead pitch and are sealed with tape. Gull-wing and J leads are available. The CHS02 and CHS10 DIP switches cost $1.74 and $2.71, respectively, in lots of 1000.



Mepcopal
11525 Sorrento Valley Rd.
San Diego, CA 92121
(800) 548-1763
▶CIRCLE 918

Buyer in Trouble #99



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"Rocky. This new catalog's not only got transformers, it's got golf balls guaranteed to go 400 yards. Don't scream, Rocky. I didn't know Prem had a new catalog. But think about it, Rocky, 400 yards... (CLICK!) Rocky?? Hello...Hello... I *really* shoulda called Prem. You oughta call Prem!"

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3521 North Chapel Hill Road, McHenry, IL 60050.
Phone: 815-385-2700. FAX: 815-385-8578.

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CIRCLE 168 FOR RESPONSE OUTSIDE THE U.S.

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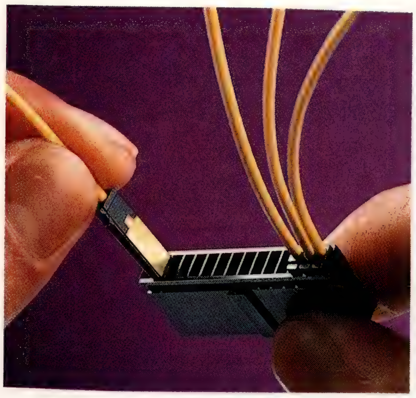
QSI CORPORATION
2212 South West Temple, #46
Salt Lake City, UT 84115 • USA
Telephone: 801-466-8770
(Fax: 801-466-8792)

CIRCLE 169 FOR U.S. RESPONSE
CIRCLE 170 FOR RESPONSE OUTSIDE THE U.S.

Controlled Impedance Ground Plane Interconnects (GPI™) are Designed to Exceed 1 GHZ System Speeds



Meritec's new Ground Plane Interconnects are engineered to match impedance and propagation rate while minimizing crosstalk. The assemblies are impedance matched from the board through the assembly to reduce signal-to-signal crosstalk. The assemblies are designed for CMOS, ECL or GaAs logic and can handle system speeds exceeding 1 GHZ with 35 pico second rise times. A spring latch connects the termination to the housing or to Meritec's Single Signal Carrier Systems (SSC™), which allow grouped interfacing with single, dual or triple row headers. Precision, high strength molded terminations are highly reliable in critical applications.

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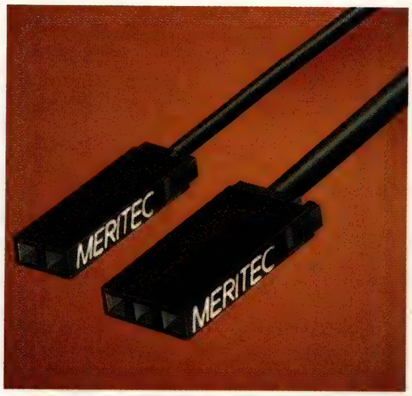
Single Signal Interconnects Offer High Performance in a Subminiature Package



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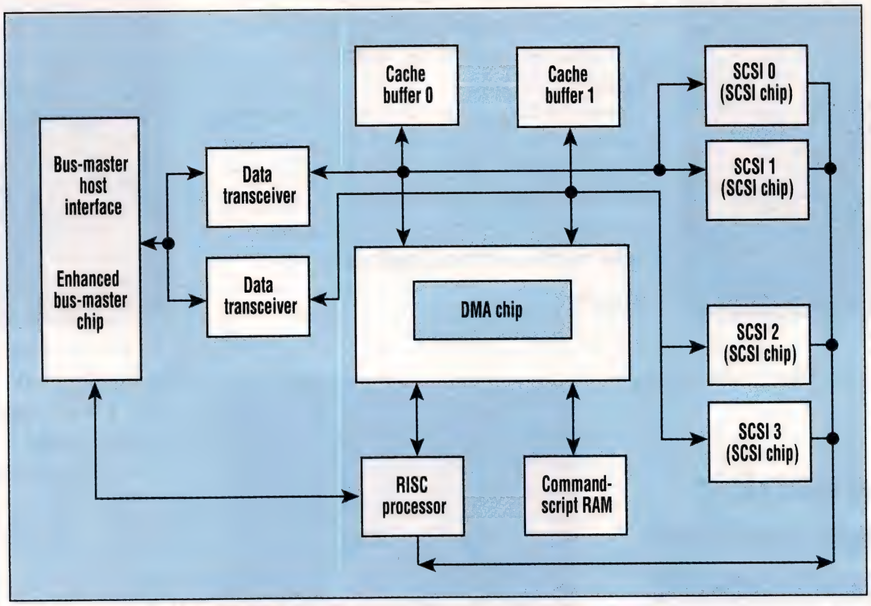
Circle 136



1. THE DMA CHIP on this controller board facilitates 40-Mbyte/s data transfers. It can handle up to eight channels and features two sets of address and control lines for communications with truly independent memory banks. Also, the chip takes the command scripts prepared by the local processor and transfers the data between the buffer memory and the system memory or SCSI channels.

SCSI Disk-Array Controller Board Handles RAID And Can Pass Data At 40 Mbytes/s.

Connect Disk Arrays To EISA Or PCI Buses

Richard Nass

Hard-disk drives are being pushed to their limit as more data moves around the computer platform or network. Disk arrays are an alternative, but that doesn't necessarily solve the problem because data must be shuttled in and out of the array at high speeds. One approach is to connect the array to a SCSI or PCI interface, but a high-speed adapter is required to completely optimize the connection from the array to the host, typically a PC LAN file server. That's where the DA-2788, DA-2988, and DA-4988 boards step in.

These high-speed disk-controller boards, developed by BusLogic Inc., work with redundant arrays of inexpensive disks (RAID). The 2788 and 2988 are two-channel boards that work with the EISA and PCI buses, respectively. The 4988 is a four-channel PCI implementation. The two-channel boards hold 14 drives, while the four-channel version handles up to 28 drives. There's no limit to the capacity of the drives as long as they employ a 32-bit logical block address, with each logical block containing 512 bytes. The three controllers support all RAID levels, including 0, 1, 3, and 5. They're configured for Novell NetWare, MS-DOS, and Microsoft Windows. Soon to come are operating-systems support for Windows NT, Unix, and OS/2.

The controllers are built with a highly integrated DMA chip that passes data between the drives and the controller at 40 Mbytes/s (although it's only 10 Mbytes/s across the SCSI interface). The controllers, which act like traffic cops, speed operation by allowing concurrent parallel data transfers. The DMA controller can handle up to eight channels. Six of the channels communicate with six SCSI buses; the other two are for host data transfers and disk-array parity calculations. Each controller also contains two sets of address and control lines to communicate with truly independent memory banks, allowing one bank to transfer data between the buffer and the system memory while the other bank moves data over the SCSI bus *(Fig. 1)*. Each bank can transfer data concurrently at a maximum rate of 40 Mbytes/s.

INTELLIGENT DMA

The DMA chip is built with intelligence, almost like a processor. It takes all of the command scripts prepared by the local processor for the DMA controller and transfers data between the buffer memory and the system memory or SCSI channels. The command script for each channel is built into local memory as an independent command. This means that the DMA controller chip can simultaneously handle up to eight command scripts per DMA channel. In addition, the local processor always knows where memory is available in the buffer so the command scripts can be set up in the local memory for each DMA channel.

When the command script is set up, the local RISC processor grants the DMA chip permission to execute it. Then the DMA chip fetches the commands and sets up an address pointer to do all of the transfers automatically. This dramatically reduces the RISC processor's overhead. As a result, the processor can spend more time managing the disk array.

Within the DMA controller is a parity buffer to implement parity logic. As a result, data can be fetched, calculated, and transferred to the buffer and all the parity fetches can be handled by the local processor.

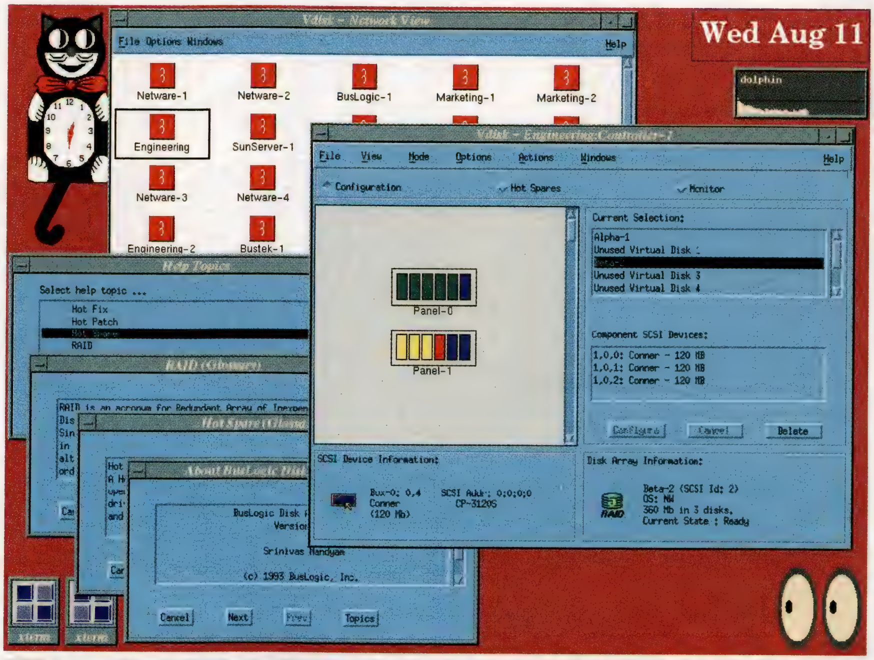
On the host side of the controller, the SCSI-channel chip handshakes with the DMA chip at 40 Mbytes/s. As a result, the DMA bus can multiplex between multiple SCSI channels without causing a bottleneck. The SCSI chip can handle 8- or 16-bit data, with the 16-bit capability allowing for an easy upgrade to wide SCSI (which operates at 20 Mbytes/s). Aside from upgrading the firmware, the only other change required when implementing wide SCSI would be to move from a 50-pin connector to one with 68 pins.

The fourth major component on the board is a bus-master chip that has ports for six buses. The chip is designed to fetch a command packet at the controller's maximum speed to minimize command overhead. It also allows data to be handled in a pipelined fashion—while one segment is being processed, the next can be set up as a stand by. As soon as the current segment is complete, the next segment starts without any setup time.

FLEXIBLE FIRMWARE

The controller's firmware must be flexible enough so that any RAID level can be employed without causing an incompatibility problem. During power-up, the firmware executes an extensive diagnostics routine, then interfaces with the on-board BIOS. This alerts the controller as to whether the array had been initialized or if it consists of raw drives. Whatever the case, the firmware prompts the user through the correct procedure.

When running in the system, the firmware emulates a host-adapter card. Thus, from an operating-system point of view, it's seen as a host-adapter card. The system doesn't know that it's connected to an array. Because of that, the firmware must



Current Selection:
Alpha-1
Unused Virtual Disk 2
Unused Virtual Disk 3
Unused Virtual Disk 4

Component SCSI Devices:
1,0,0: Conner - 120 MB
1,0,1: Conner - 120 MB
1,0,2: Conner - 120 MB

Select help topic ...
Hot Fix
Hot Patch
RAID

SCSI Device Information:
Bus-0: 0,4 SCSI Addr: 0;0;0;0
Conner CP-3120S
(120 Mb)

Disk Array Information:
Beta-2 (SCSI Id: 2)
OS: NW
360 Mb in 3 disks,
Current State : Ready

RAID is an acronym for Redundant Array of Inexpen

BusLogic Disk
Version

Srinivas Nandyam

(c) 1993 BusLogic, Inc.

2. A GRAPHICAL USER INTERFACE IS BUNDLED with BusLogic's DA-2788, DA-2988, and DA-4988 controller boards. The interface is divided into local and network levels. Each node on the network is represented by an icon and a name. From this screen, the user can gain configuration information or monitor the status of each node on the network.

be able to handle all of the host-adapter card's features as well as interface to all device drivers without any modification. Because the firmware is incorporated into the host adapter, a separate controller board is eliminated.

A feature of the controller is its ability to swap drives without powering down the array (hot swapping). The firmware periodically scans every drive to detect errors. If an error occurs, the user is notified immediately. If a hot swap is needed, the firmware can reissue all of the current pending commands, thus maintaining data integrity.

EASY INSTALLATION

The configuration utilities are designed so that if the user isn't familiar with disk arrays, the installation goes through a default setup. There's an optimized set of default parameters for each operating system. After entering the correct operating system, the hardware will configure itself. If users have experience with disk arrays, they can fine-tune each parameter. Then initialization starts, giving each drive the proper parity.

The entire installation process actually takes under a minute. Initialization only has to be done once. After that, the system will boot automatically. Once the system is booted, a user interface is activated, which, depending on the operating environment, is either character- or graphically-based.

The graphical interface is divided into two segments—a local level and a network level. Each node on the network is represented by an icon and a name *(Fig. 2)*. For example, if a company had a different array for each department, each would require a separate node at the network level.

To access information about a node on the network, the user just double clicks on that icon. From this screen, the operator can either change the configuration or monitor the status. The user screen is configured such that when a failure occurs, the user is immediately alerted. The network-management software lets users monitor any node on the network from any other node, regardless of the operating system. Users can even monitor nodes across different operating systems.☐

PRICE AND AVAILABILITY

The two-channel EISA board (DA-2788) sells for $1495. The two- and four-channel PCI boards (DA-2988 and DA-4988) go for $1795 and $2095, respectively. All will sample in the first quarter of next year, with production starting in the second quarter. Controllers for Micro Channel, the VL-Bus, and a four-channel EISA version will soon follow.

BusLogic Inc., 4151 Burton Dr., Santa Clara, CA 95054; (408) 492-9090.

CIRCLE 525

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SLIGHTLY	567

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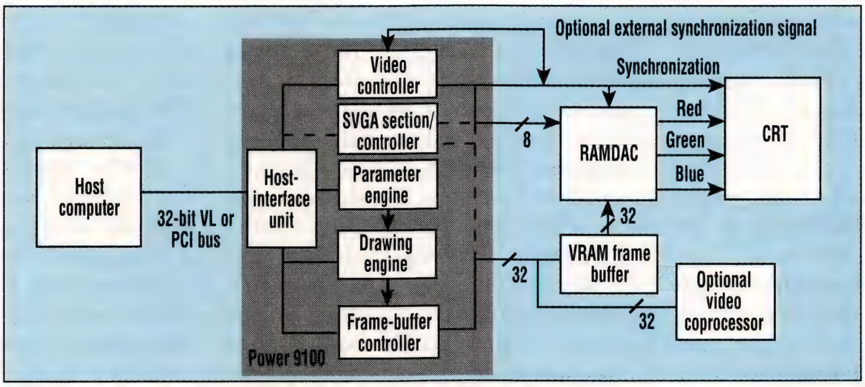


WITH AN ON-CHIP DRAWING ENGINE, VL and PCI-bus interfaces, and SVGA and frame-buffer controllers, the Weitek Power 9100 is able to deliver over 25 million WinMarks at 24 bits/pixel. The controller/accelerator requires only an external RAMDAC, a VRAM-based frame buffer, and, as an option, the Video Power coprocessor to enhance digital-video multimedia applications.

A GRAPHICS CONTROLLER AND ACCELERATOR GIVES PCS THE LOOK AND FEEL OF A WORKSTATION.

CHIP SET DELIVERS FAST GRAPHICS, DIGITAL VIDEO

DAVE BURSKY

As more and more programs depend on high-resolution graphical user interfaces such as Windows, OS/2, Windows NT, etc., the graphic display subsystem becomes one of the computer's performance bottlenecks. Screen resolutions and colors are now achieving 1280-by-1024-pixel resolutions with 24-bit true color, or 1600-by-1280-pixel resolutions with 16-bit color, so moving pixels on the screen must be done quickly. However, bringing up fresh data from memory or performing window movements requires not only high-speed buses like the VESA VL-bus or the Peripheral Component Interconnect (PCI) bus, but also high-performance controllers/accelerators.

Both high-performance buses and acceleration logic have been unveiled during the last couple of years, with each generation bringing slightly higher resolution and faster image movement. Now Weitek has come up with the Power 9100 controller/accelerator IC and the Video Power coprocessor, a two-chip moderately-priced solution that can give VL- or PCI-bus PCs graphics and digital-video performance typically seen on RISC workstations. Furthermore, the coprocessor supports multiple video data streams, which suits the circuit well for handling video-conferencing applications.

The Power 9100 controller can accelerate 8-, 15-, 16-, 24-, and 32-bit/pixel transfers, and draw lines and polygons at full video-RAM (VRAM) bandwidths. The 208-lead chip also performs bit-block transfers (bitBLTs) from screen to screen at the full VRAM bandwidth, and from host to screen (with color expansion) at up to 50 MHz (200 Mbytes/s with a 32-bit interface).

The companion 160-lead Video Power circuit adds multimedia video capabilities to the graphics system, with full-screen TV-quality video playback of images and with resolutions of up to 1280-by-1024 pixels at 30 frames/s. Furthermore, the coprocessor provides a seamless interface since the chip's features are accessed at the graphical-user-interface device-driver level, not at the application level.

The Power 9100 contains a super VGA controller, a drawing engine, frame-buffer control logic, and VESA VL and PCI host-bus interfaces. The controller supports either 32- or 64-bit-wide RAMDACs at speeds of up to 200 MHz *(see the figure)*. In one configuration with 4 Mbytes of video memory, rather than the 8 Mbytes previously needed, the Power 9100 can run fully accelerated 24-bit true-color displays with resolutions as high as 1280 by 1024 pixels, and deliver a throughput of more than 25 million WinMarks at 24 bits/pixel—not the 8 bits/pixel typically quoted (WinBench version 3.11 on a 60-MHz Pentium VL-bus system).

In contrast, the company's previously released Power 9000 controller is optimized for 8-bit color and thus delivers only about 8 million WinMarks in true-color mode, but delivers 60 million WinMarks in the 8-bit color mode. The simpler circuit doesn't include the SVGA controller, the VL and PCI bus interfaces, or the ability to fully accelerate 24-bit color. Since its original release, the Power 9000 driver software has been improved such that the newest versions deliver a 50% performance boost over the initial release. A companion chip, the Power 9001, provides a PCI-bus interface, simplifying PCI-compatible card design with the lower-cost Power 9000.

By adding the Video Power chip for a small incremental cost, systems based on the Power 9100 can have full-screen, 30-frame/s digital video rather than the quarter- or eighth-screen-size (320-by-240-pixel or 160-by-120-pixel) and 10 to 15 frames/s typically available with software-only schemes. The circuit also supports all the leading compression/decompression formats, including Intel's Indeo, Supermac's Cinepak, Media Vision's Captain Crunch, MPEG, and motion JPEG.

To handle all the popular formats, designers at Weitek found a set of common functions that could be integrated on the coprocessor—interpolative scaling, color-space conversion, and dithering. By implementing those functions in hardware, digital video can produce high-quality full-screen (1280-by-1024-pixel and 24-bit color) images at 30 frames/s. Furthermore, they added a two-channel frame-buffer controller—one channel handles the on-chip pixel processor and the other channel supports the VESA Media Channel.

To deliver the 25 million-plus WinMarks with 24-bit color, the Power 9100's internal drawing engine provides automatic clipping against window and screen edges, and supports patterning, plane masking, and Boolean operations on pixels during drawing. A directly-mapped linear frame buffer allows the CPU to efficiently access frame-buffer memory without banking schemes.

At the heart of the Power 9100 lies both a parameter engine and a drawing engine. The parameter engine prepares drawing operations for execution by the drawing engine. It takes input coordinates from the host and converts them to a form usable by the drawing engine. Input parameters include the X and Y vertices of polygons, and the corners of bitBLT regions. The parameter engine tests the vertices against window and screen boundaries, tests for exceptions, and performs trivial rejection. Finally, it transfers commands that pass these tests to the drawing engine, which then renders the command into the frame buffer.

Working independently of the drawing engine, the parameter engine can accept parameters for a new operation while the drawing engine is busy executing the previous command. Four types of polygons are prepared by the parameter engine—quadrilaterals, triangles, lines, and points. Furthermore, the engine coordinates bitBLTs from screen to screen or from host to screen.

Once a command is passed to the drawing engine, the drawing engine does three basic tasks—it draws quadrilaterals (the quad operation), triangles, lines, or points; it performs screen-to-screen bitBLTs; and it performs host-to-screen bitBLTs. The quad operation treats triangles, lines, and points as special cases of the quadrilateral (a quadrilateral with one or more identical vertices).

These "special cases" can always be rendered correctly. The drawing engine, though, is unable to draw convex quadrilaterals in a horizontal position (bow tie format), but can draw them vertically (hourglass appearance). However, even though bow-ties can't be drawn directly, driver software typically decomposes the image into two triangles.

Screen-to-screen bitBLTs are very straightforward, with the drawing engine just copying a rectangular area of the display from one screen location to another. Two choices exist within the host-to-screen bitBLT mode: Pixel1 and Pixel8. The Pixel1 operation takes monochrome, 1-bit/pixel data from the host, expands the pixels internally to the current pixel depth (typically by assigning the foreground and background colors to One and Zero bit states), and writes the bits to the frame buffer. Up to 32 pixels can be transferred to the Power 9100 in a single word. The Pixel8 operation takes in color pixels with depths of 8, 16, or 32 bits, packed as four, two, or one pixel/word, respectively, and writes them to the frame buffer.

The use of a dual-ported VRAM-based frame buffer maximizes system performance. Although a VRAM is more expensive than a DRAM, the dual ports allow the pixel-data-output port to update the display while new data is transferred in through the memory's random-access port. Two banks of VRAM can be interleaved to maximize video-memory data transfers, yet they eliminate the need to use wide, 64-bit buses. As a result, system bus overhead is minimized.

By sharing the frame buffer, the Video Power chip can send its images directly to a display window—that reduces both cost and system complexity while maximizing system performance. The circuit also supports the VESA Media Channel, a peer-to-peer multi-master bus standard for real-time data streams. The channel allows more multimedia hardware to be added to the system.

Included on the coprocessor is an interpolative scaling engine that employs two-dimensional digital filtering to size the images to any desired size. Interpolation provides better quality than the more-commonly used pixel-replication schemes. Scaling resolution is 1/4096 of the input pixel spacing while accuracy is to within 1/8 of an input pixel space.

Additionally, the circuit performs color-space conversion from all popular formats—YUV 4:4:4, 4:2:2 (CCIR 601), 4:1:1 (CCIR 601), 4:2:0 (MPEG), 4:1:0 (Indeo YUV9), and both packed RGB and YUV 16 (4:2:2)—and delivers grey-scale or 8-, 15-, 16-, 24-, or 32-bit RGB color outputs. If desired, on-chip dithering logic converts from 24-bit true-color to dithered 8-, 15-, or 16-bit color. Additionally, a bitBLT engine on the coprocessor moves the images to the frame buffer at up to 200 Mbytes/s.

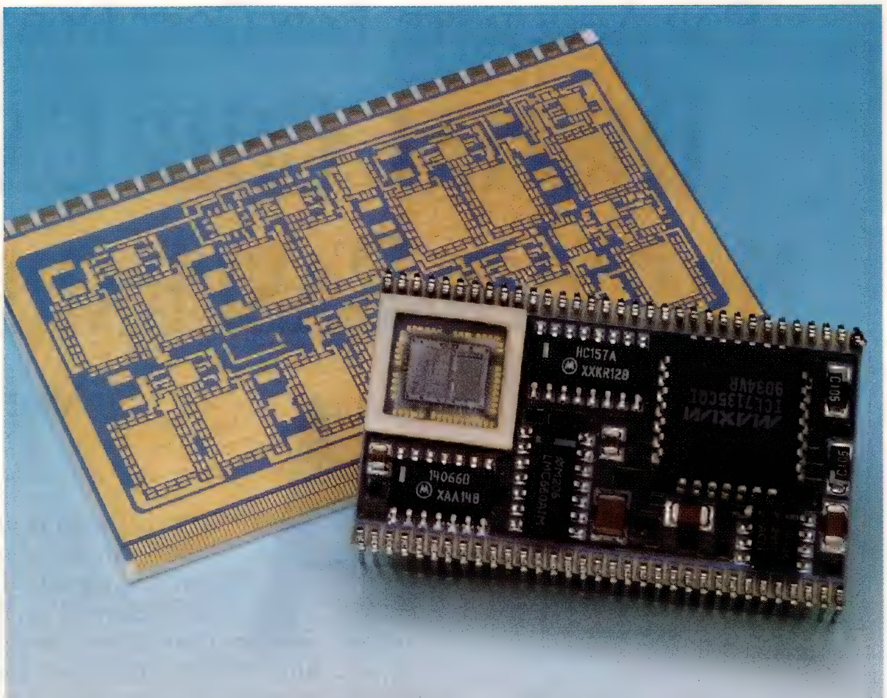
Because the Power 9100 provides a glueless interface to the host VL or PCI buses, it only requires the RAMDAC and frame buffer to complete the video subsystem. The optional Video Power coprocessor can be added to accelerate and enhance digital video for multimedia applications. Finally, the Power 9100 supports the VESA-defined power-management specification, which will help systems built with the chip minimize standby power dissipation. Driver software for Microsoft Windows, Video for Windows 1.0 and 1.1, Windows NT, and OS/2 2.1 Ultimotion, SCO Unix, Microstation, and AutoCAD, plus extra program-specific drivers, are available from Weitek.☐

PRICE AND AVAILABILITY

The Power 9100 graphics controller/accelerator comes in a 208-lead PQFP. In production quantities, it will sell for about $85 each. The 160-lead PQFP-housed Video Power coprocessor chip sells for $30 apiece, also in production quantities. The 208-lead Power 9000 and its companion 160-lead Power 9001 sell for $45 and $18 each, respectively, in production quantities. Samples are available from stock.

Weitek Corp., 1060 E. Arques Ave., Sunnyvale, CA 94086; Bob Butchko, (408) 738-8400. CIRCLE 513

HOW VALUABLE?	CIRCLE
HIGHLY	544
MODERATELY	545
SLIGHTLY	546



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CMOS IC COMBINES FREQUENCY SYNTHESIS, MIXING, AND FILTERING FUNCTIONS FOR ACCURATE, LOW-COST DOWN-CONVERSION.

DIGITAL CHIP CAPTURES NARROW-BASEBAND SIGNALS

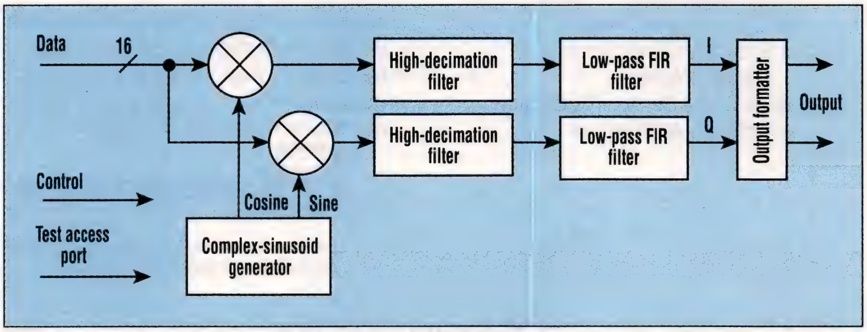
MILT LEONARD

A key challenge in designing a radio receiver for a wireless data-communications system involves extracting the narrowband signal of interest from a wideband IF input. Called down-conversion, this function historically has been served by expensive board-level analog solutions with limited precision. More recently, designers have turned to full-custom digital-signal-processor boards costing thousands of dollars.

But these solutions don't qualify for cost-sensitive, space-limited applications like cellular telephones, wireless local-area networks, and satellite communications. For such applications, Harris Semiconductor has developed a DSP chip with a 52-Msample/s input sampling rate, the HSP50016, which can be configured for a range of end-system requirements. The device is made on a submicron CMOS process with three levels of metal.

The HSP50016 digital down-converter (DDC) consists of a frequency synthesizer, a quadrature mixer, and two low-pass filters *(Fig. 1)*. The circuit can tune in center frequencies with a resolution of under 0.009 Hz and mix with an internal local-oscillator signal over a 102-dB spurious-free dynamic range. Also contributing to the chip's accuracy are a passband ripple of under 0.04 dB and stopband attenuation in the filters of over 106 dB.

The DDC's parallel input port accepts the real component of an input data stream from an external analog-to-digital converter. This data stream is then multiplied by a complex sinusoidal waveform whose frequency is programmable from dc to one-half the input sample frequency ($f_s/2$). The chip then performs down-conversion, narrowband low-pass filtering, and decimation from 64 to 131,072 to produce a baseband signal.



1. THE HSP50016 DIGITAL DOWN-CONVERTER captures a narrow frequency band of interest from a wideband input, converts that band to baseband, and delivers it in quadrature or real form. Consisting of a complex sinusoid generator, a phase generator, and mixers, the internal synthesizer can produce continuous-wave, frequency-hopped, or linear frequency-modulated up-chirp and down-chirp waveforms. Output data can be single-precision floating-point or fixed-point arithmetic in 16-, 24-, 32-, or 38-bit two's-complement, signed-magnitude, or offset-binary formats.

The internal synthesizer can tune in on various signal forms, including frequency-hopped and swept sine waves. The complex result is low-pass filtered and decimated with identical real-component filters in the in-phase (I) and quadrature-phase (Q) processing chains. A high decimation filter followed by a fixed decimation finite-impulse-response filter performs low-pass filtering.

The combined response of the two-stage filter produces a shape factor of 1.5 (from –3 dB to –102 dB). Composite bandpass ripple is under 0.04 dB.

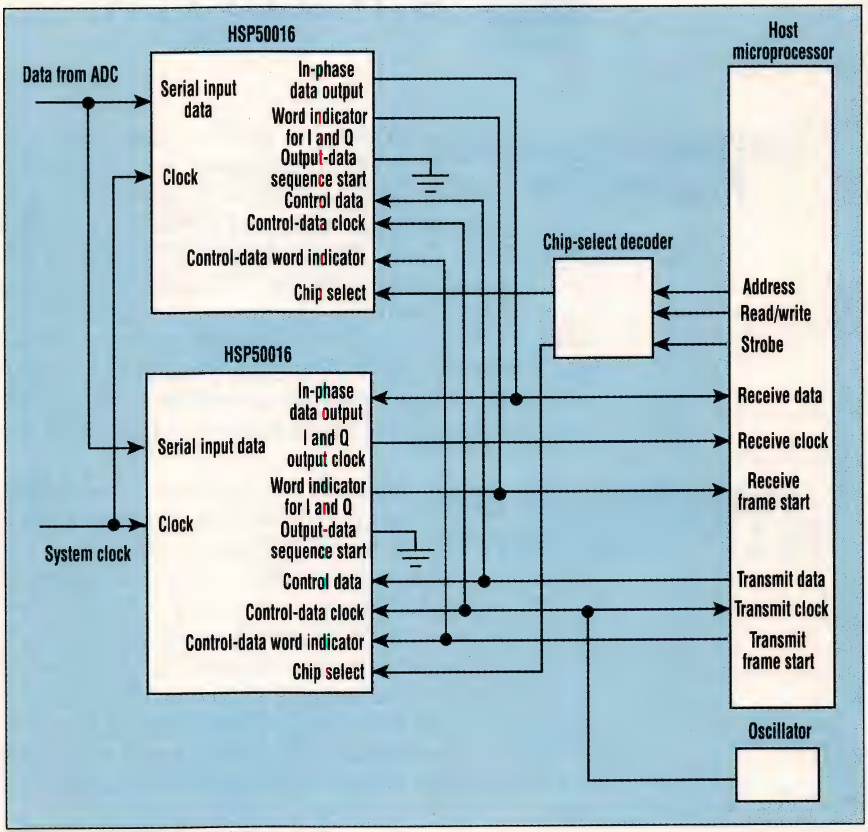
Eight 40-bit serial command words control the chip, which can read at rates of up to 10 Mbits/s. The outputs include a stream with the real component of the data or a complex-quadrature data stream in serial format. The baseband output signal can be demodulated by any standard DSP IC. The amount of processing required for demodulation is reduced by the choice of upper or lower sideband at the chip's output.

Beyond a programmable sample rate of 52 MHz or less, the HSP60016 is flexible in other areas. A user can set the center frequency for either a constant value or a chirp. The chirp is a swept frequency where the user sets the start, stop, and rate-of-change of the center frequency. The width of the output-frequency band is also programmable. Output-signal choices include 16-, 24-, 32-, or 38-bit fixed-point or IEEE floating-point arithmetic. Output data formats can be real or complex data, simultaneous or sequential I and Q data, and normal or spectral-reversed data. The output frequency spectrum can be centered at about $f_s/2$.

SYSTEM IMPLEMENTATION

Applying the HSP50016 is fairly straightforward. Only six wires are required to interface the chip to any standard DSP IC that executes the demodulation function. The external wire count is limited to connections for serial line data, a clock signal, and a strobe signal. Designers can bus multiple HSP50016s in parallel, with each one operating on a different frequency band. In this case, the wiring is simplified by connecting the outputs of each HSP50016 over a common serial bus *(Fig. 2)*. Each DDC is assigned a time-slot number and a time-slot length. In turn, each DDC controls the bus long enough to deliver its data before relinquishing the bus. The time-slot assignment and length are programmed during system configuration. Up to 64 chips can be multiplexed in this manner.

Alternatively, the host processor can request data from each DDC asynchronously. This mode requires a data concentrator (a user-designed custom circuit), which polls each channel individually and ensures that all channels are polled before the output data is lost. An IEEE 1149.1 JTAG (Joint Test Action Group) test-access port is included for military applications.



2. UP TO 64 HSP50016s, each operating on a different frequency band, can be connected in parallel and multiplexed over a common serial bus. Collisions are avoided by programming a different time slot for each device. This example shows all digital down-converters in the I-followed-by-Q mode, which requires just one data line to the microprocessor.

Each HSP50016 replaces two analog filters, a frequency synthesizer, and two mixers. An alternative discrete digital solution would require a numerically controlled oscillator (NCO), several multipliers and filters, plus discrete logic for configuration and control. An ASIC solution would raise cost, risk, and time-to-market issues.

In one chip, the HSP50016 executes down-conversion functions that formerly required three Harris ICs: the HSP45116 NCO modulator (NCOM), an integrated quadrature NCO and high-speed complex multiplier/accumulator, and two HSP43220 decimating digital filters (DDFs). According to Harris, designers may find the DDC more appropriate than the NCOM/DDF combination for narrowband applications (decimation of 64 or more), while the NCOM/DDF combination may be better suited for applications requiring programmable filters.

Harris plans to provide a serial I/O filter for use with the DDC. By cascading two such ICs, designers can implement a programmable FIR filter to further enhance the DDC's flexibility. The HSP50016 is available in a 48-pin PGA, a 44-pin PLCC, and a 48-pin PQFP.☐

PRICE AND AVAILABILITY

The HSP50016 digital down-converter is available now at a starting price of $80 each in quantities of 1000.

Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901; 1-800-4-HARRIS, ext. 7083. **CIRCLE 511**

HOW VALUABLE?	CIRCLE
HIGHLY	533
MODERATELY	534
SLIGHTLY	535

PRODUCTS NEWSLETTER

UNIVERSAL PROGRAMMER FEATURES LOW PRICE

Priced at a level to allow companies to equip all engineers with their own device programmer, the ChipLab Project Programmer from Data I/O Corp., Redmond, Wash., is a prototyping tool for programming memory, microcontroller, programmable logic, and FPGA devices. Technologies supported by the prototyping tool includes Flash, PROM, E/EEPROM, PALs, GALs, Mach, and Max. Besides DIP packages, ChipLab accommodates surface-mount packages such as PLCC, SOIC, QFP, and TSOP, using optional adapters. The unit works with any 286, 386, or 486 PC or PS/2-compatible computer, and features a Windows-like software interface with simple pull-down menus. The interface allows quick device selection with multilevel filters, including device category, manufacturer, and part number, as well as extensive on-line help. Suggested list prices for ChipLab are $895 for the 32-pin version and $1495 for the 48-pin version. *JN* **CIRCLE 888**

SYSTEM SIMULATOR RUNS ON A PC UNDER WINDOWS

SystemView, a system simulator from Elanix Inc., Westlake Village, Calif., can handle both analog and digital systems. The simulator, which runs on PCs under Windows, consists of a high-level conceptual design and analysis engine embedded in an intuitive, graphical design environment. Engineers use symbolic tokens to represent various processing elements, and then connect them to form a complete system in the software's design window. The only typing required is parameter-data entry, such as a filter's bandwidth. SystemView libraries contain many different filters, logic functions, switches, and more. An interactive analysis window allows users to examine system waveforms with zoom, scroll, and filtering functions. Targeted applications include signal processing, communications, and general mathematical modeling. SystemView is shipping now for less that $1000. Call (818) 597-1414 for more information. *LM* **CIRCLE 889**

PRICING CHANGED FOR LOGIC-SYNTHESIS TOOLS

The logic-synthesis tools from Exemplar Logic Inc., Berkely, Calif., are now available in different product configurations with reduced pricing. Exemplar's Core product family can synthesize complex PLDs, FPGAs, and ASIC devices. The most significant repackaging change is the combined Verilog-VHDL front end, which is sold bundled with the company's top-down tool suites. The 'x'pediter Series is a DOS-based product line for users just getting started in logic synthesis. It features flexibility, intuitiveness, and ease of use at pricing between $5000 and $8000. The more robust 'x'plorer Series is for Unix-based designers who typically have more experience with logic synthesis. That product line costs between $15,000 and $30,000. Within each of the two series there are separate tool suites aimed at either design migration or top-down design. Call the company at (510) 849-0937 for more details. *LM* **CIRCLE 890**

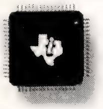
DSP CORE, SOFTWARE TARGET COMMUNICATIONS

A pair of licensing arrangements gives Silicon Systems, Tustin, Calif., and Xicor, Milpitas, Calif. access to Pine, a high-performance integer DSP core. Also licensed by Silicon Systems are the rights to the Truespeech audio compression algorithms. The Pine DSP core and the Truespeech algorithms were developed by The DSP Group, Santa Clara, Calif., and its subsidiary, DSP Semiconductors USA. Silicon Systems expects to incorporate the Pine DSP core into a wide range of low-power, low-profile communications ICs that support the LAN, modem, wireless, and multimedia product areas. Such developments extend SSI's many communication products, which the company developed along with a wide range of expertise in algorithms, protocols, and mixed-signal circuit design that now complement the DSP core. With its 15:1 compression ratio, DSP's Truespeech algorithm squeezes a 1-min. voice file down to just 60 kbytes with no noticeable voice-quality degradation—other compression schemes need up to 940 kbytes for the same quality. Used by companies selling tapeless telephone-answering machines, Truespeech was recently selected to be included in some Compaq and Microsoft products. Planning to apply its programmable logic expertise to supplement the functionality of the Pine DSP core, Xicor will develop products that combine the DSP core and programmable logic to create the first field-configurable DSP-based logic chip. Call Ed Larc, Silicon Systems, (714) 573-6200; Asaf Mohr at the DSP Group, (408) 986-4300; or Raphael Klein at Xicor, (408) 432-8888. *DB* **CIRCLE 891**

Edited by Clifford Meth

Which converter delivers twice the speed at half the power consumption in half the height?

TI's TLC320AC01 analog interface circuit.



The new TLC320AC01 analog interface circuit (AIC) from Texas Instruments, a complete data acquisition system on a chip, supports your most demanding portable and voice-band applications.

The 'AC01 is a fully programmable device that integrates 14-bit A/D and D/A converters, filters and I/O for a complete analog interface system.

The device combines twice the conversion speed with half the power consumption in half the height of TI's previous generation of AICs. This new generation is enabled by TI's advanced mixed-signal design methodology and 1-micron processing technology.

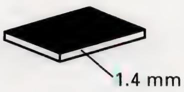
The 'AC01 interfaces directly with TI's leadership TMS320 digital signal processors (DSPs) and with other industry-standard DSPs and most general-purpose microprocessors.

And it can operate in three modes — stand-alone, master-slave and linear codec — for greater system-level design flexibility.

The 'AC01 can enhance the performance of your V.32 bis modem and PCMCIA card, speech and audio processing including multimedia, noise cancellation, industrial control and instrumentation designs.

TLC320AC01 At A Glance

- Low power consumption (100 mW) for portable systems
- Direct serial interface to most DSPs
- Shrink quad flat packaging (SQFP) available for low-profile, portable applications



- Single 5-V power supply for simplified system design
- 14-bit A/D and D/A converters and programmable filters
- Signal-to-distortion ratio: 72 dB
- TLC320AC01CFN 28-pin PLCC; TLC320AC01CPM 64-pin SQFP

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TI's new generation of analog interface circuits. For more data, just return the reply card, call your local TI sales office or fax us at **886-2-377-1460.**

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"Increasing our ad budget was so successful, our agency recommended we cut it."

Photo: Frank Moscati

See what it's like to live 7 days without tranquilizers.
True, Columbus paid less than $945 getting to the Caribbean, but he had to take the Nina, the Pinta and the Santa Maria.
Sometimes you just gotta stop and smell the saltwater.
If you've never been early for anything in your life, it's probably because nobody made it worth your while.
With prices like these, you'd probably expect to row.
The last time the launching of a ship got this much attention it rained for 40 days and 40 nights.
The only thing standing between you and our cruise to Bermuda is $895 and an occasional pothole.
Once a year the swallows fly to Capistrano. The salmon swim to their spawning ground. And Floridians cruise to Bermuda.
It's like Monty Hall putting the big deal behind all three doors.
Sure, you could crawl in a hole and hide. But wouldn't our bright spacious cabins be more comfortable?

Al Wallack, Sr. VP Marketing, Celebrity Cruises, after returning from having his hearing checked.

"A great time to introduce a new luxury cruise line. The economy was in a slump, and the competition was on the rise.

We told our new advertising agency we have to go in with all guns blazing. And gave them the extra money to do it.

They recommended a three phase campaign. Phase 1. Full page newspaper. One ad a week for 24 weeks and one-third pages in the travel section. Phase 2, radio. Then 3, television to sweep up one season and sow the seeds for the next.

To make a long story short, two-thirds into the newspaper phase, Celebrity's ships were just about full to the end of the season. With so little left to sell, we all agreed to hold the radio and TV and save the remainder of the budget.

In roughly two years Celebrity became the number one cruise line from New York to Bermuda.

We've just added another new luxury ship and we're anxious to fill it. So once again we've upped our budget. So far, our agency hasn't tried to talk us out of it."

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This advertisement prepared by Korey, Kay & Partners, New Yor

AT-BUS-SYSTEM 160-LEAD CHIP SET FEATURES VL-BUS INPUT/OUTPUT OPTION AND POWER-MANAGEMENT FEATURES

By integrating the motherboard logic for 486-class "SL-enhanced" systems, the Wagner chip set provides a VL-bus interface as well as power-management features that lets systems meet EPA "Green" PC standby power levels. The two 160-lead chips, developed by Symphony Laboratories, form the heart of the motherboard and can be used in either desktop or portable systems.

The Wagner chip set requires just seven simple TTL chips to complete the basic motherboard design. In contrast, some other solutions offer a single-chip controller, but those solutions typically require anywhere from as little as 17 and as much as 22 TTL support chips.

Targeted at systems that employ Intel's 486 SL enhanced power management or other central processing units with system-management modes, the Wagner chip set provides four operating modes. Those modes are full on, CPU standby, global standby, and suspend. Each of these modes successively reduces the system's operating power level to keep within the 30-W target level called for in the Energy Star program.

The chips provide SMI support for background control, stop-clock logic to reduce idling power, and both activity detection and an activity time-out timer. Systems using either 5-V or 3.3-V power supplies, or a combination of both, can be built with the Wagner chip set.

To provide a high-speed I/O capability in addition to the standard ISA (AT-bus), the Wagner chips also can drive up to three VL-bus-master card slots.

The SL82C491 main memory and cache controller can address up to 256 Mbytes of main memory (four banks) and up to 1 Mbyte of burst-mode cache, which can be organized as either write-back or write-though.

The companion SL82C492 chip contains the power-control logic circutry, the SMI support circuitry for up to 128 kbytes of system management software, and other resources—two 82C59A interrupt controller chips, two 82C37A DMA controller chips, and one 82C54 timer IC.

In quantities of 10,000 sets, the two-chip Wagner chip set sells for $16 per set. Samples of the chips are available from stock.

Symphony Laboratories, *4000 Burton Drive, Santa Clara, CA 95054; Jack Yuan, (408) 986-1701.* **CIRCLE 930**

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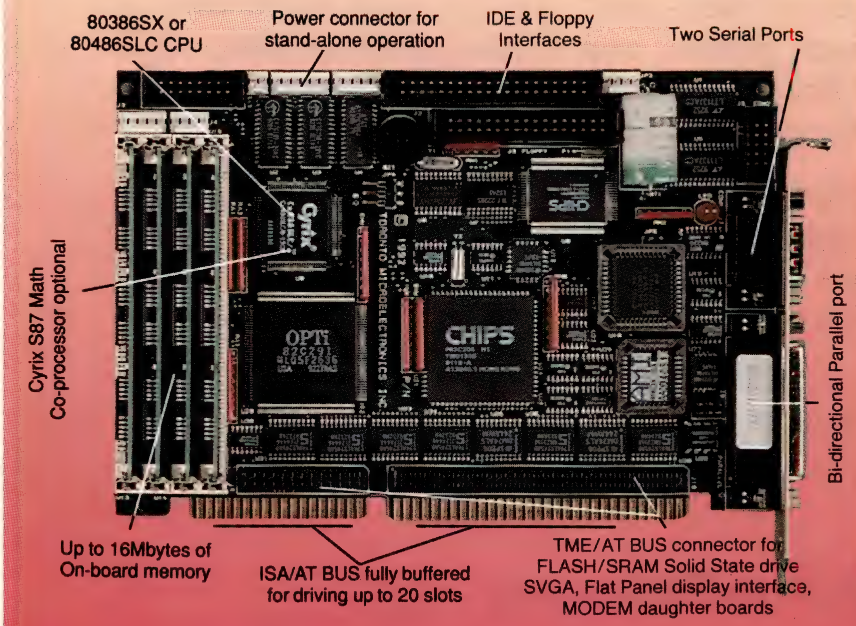
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TME/AT BUS connector for FLASH/SRAM Solid State drive SVGA, Flat Panel display interface, MODEM daughter boards

TME's F486SLC		COMPETITOR
✓	80386SX	Yes
✓	80486SLC	?
✓	16/25/33/40Mhz	?
✓	Up to 16 Mbytes of On-board memory	Yes
✓	64K Write back cache	No
✓	Two serial ports with 10KV ESD Protection	No
✓	One Parallel Port	Yes
✓	Floppy & IDE interface	?
✓	Under 6.5W capability	?
✓	Watch Dog Timer	?
✓	Power Fail Detection	No
✓	Small form factor 4.75" x 7"	?
✓	Optional FLASH/SRAM Solid state drive, Flat panel display, VGA & SVGA interfaces	?
✓	Fully buffered AT BUS for driving up to 20 slots	No

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PENTON CONTINUES COMMITMENT TO RECYCLING

Penton Publishing's Camera Department started recycling chemicals from film wastewater 25 years ago... long before the ecologically-smart idea was widely recognized.

For almost as many years, the Penton Press Division has been recycling scrap paper, obsolete inventory, and printing press waste materials. In 1991, Penton Press will recycle some 5500 tons of paper, 9 tons of aluminum plates, and 3 tons of scrap film negatives. Furthermore, the Press Division has invested $500,000 in air pollution control equipment.

Company-wide, the recycling spirit has spread from Cleveland headquarters to offices throughout the country. Penton employees are enthusiastic participants in expanding programs to re-use paper, aluminum cans, and other waste materials.

Penton Publishing believes these practices make a significant quality-of-life difference for people today... and will help create a safer, healthier environment for generations to come.

Penton Publishing

386-COMPATIBLE CPUS FILL EMBEDDED NEEDS

The 80386 microprocessor made significant inroads into control and industrial applications. But unlike Intel's 80186 and 80188 highly integrated processors based on the 8086 core, the 80386 needs many support chips as it wasn't designed for control applications. Now Intel has ended the need for an array of support functions with a high-integration version of the 80386: The 386EX contains many of the same support functions as the 80188 but also has a static 386SX core, power-management logic that offers three low-power options (idle, powerdown, and powersave), and the system-management mode for background operation control. Thus, the 386EX can upgrade systems currently using 80186/80188 type processors.

The 386EX also retains DOS compatibility, so designers can easily transfer over programs that were developed on PCs. The 80188 and 186 aren't directly DOS compatible, so many I/O control routines were modified or special software traps were set up to catch the improper references. On-chip resources reducing the need for off-chip support include three counter-timer channels, two DMA channels, a DRAM refresh controller, up to 24 parallel I/O lines, two asynchronous serial I/O channels, one synchronous serial channel, an interrupt controller (equivalent to two 8259As), and a watchdog timer.

In addition to the 386EX, which should sample late in the second quarter of 1994, two static CMOS 386 CPUs were unveiled and are available now. The first, a standard 5-V 386SX processor built with static CMOS logic, runs at 16, 20, or 25 MHz. The chip drops into existing 386SX applications, replacing the dynamic-logic processor and reducing the idle power of such systems.

The other CPU, the 386CX, is a 386SL-like CPU in the 386SX pinout that can operate at 12 or 20 MHz when powered by 2.7-to-5.5-V supplies. Intel will also provide a royalty-free real-time incorporation license with every CX or EX processor, so users can incorporate without charge any "derived works" based on Intel's updated iRMX EMB real-time operating system, which designers can also purchase.

The static 386SX and CX CPUs come in 100-lead PQFPs; the 386EX will come in a 132-lead PQFP. In lots of 5000, the three CPUs start at $26, $27.30, and $39, respectively. Bare chips will also be available.

***Intel Corp.**, Literature Center, Box 7641, Mt. Prospect, IL 60056-7641; (800) 628-8686; (408) 765-8080.* **CIRCLE 931**

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PALETTE DACs DRIVE TOP-PERFORMING GRAPHICS IN PCs OR WORKSTATIONS

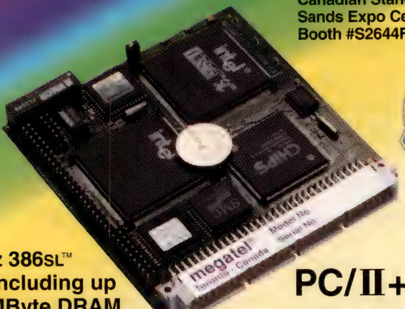
DAVE BURSKY

With top pixel data rates of 250 MHz, a family of three palette DACs can deliver data at the speeds needed to fuel top-performing true-color graphics displays. The RGB561, 530, and 525, were developed by IBM Microelectronics to drive displays with resolutions up to 1600 by 1280 pixels. Fabricated in a 0.8-μm CMOS process, the palette DACs operate at 3.3 V and include on-chip clock generators and wide graphics-memory video RAM interfaces. That interface starts at 200-bits wide for the high-end RGB561, drops to 96-bits wide for the mid-range 530, and shrinks to 64-bits wide on the RGB525. Those wide buses allow the DACs to transfer data at rates of 2.5, 1.2, and 0.8 Gbytes/s over the video-memory interface.

The low-end RGB525 has the performance of the best palette DACs used in the PC add-in cards. And performance only increases with the other two palette chips, which deliver workstation-class throughputs and features. Though all three DACs will be available in 1994 with the 250-MHz top speeds, initial versions will offer top speeds of 170 MHz, which can handle high-resolution images of 1280-by-1024 pixels with non-interlaced monitors running at up to 75 Hz. The 250-MHz chips will handle 1600-by-1280-pixel images with refresh rates of up to 90 Hz (or any combination of 2 Mpixels).

To solve many system integration and noise problems caused by high-frequency clocks, each chip integrates programmable clock generators. The PLL-based clock circuits accept 4-to-64-MHz inputs and deliver 170-to-250-MHz outputs. The RGB525 was optimized for graphical user interfaces such as IBM's OS/2 and Microsoft's Windows and Windows NT. On chip are triple 256-word-by-8-bit palette RAMs and triple 8-bit monotonic digital-to-analog converters. The DACs generate 15-, 16-, 24-bit direct color, gamma-corrected color, or provide 8-bit, 256-shade grey-scale images. The palette chip can also display a 24-bit color border and supports 24-bit packed pixels or 4-, 8-, 16-, 24-, or 32-bit pixels. On-chip cursor logic supports up to a 64-by-64-pixel cursor. The 64-bit-wide pixel data path and packed pixel mode lets the palette DAC display true-color images with 1280 by 1024-pixel resolution with only 4 Mbytes

(continued on next page)



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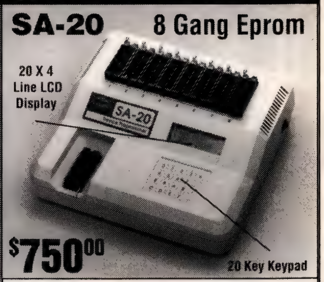

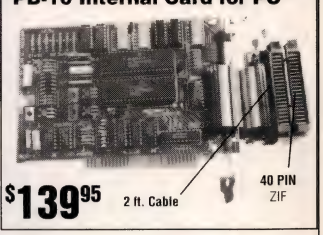

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of video memory—half the typically requirement of other palette chips.

Widening the video pixel bus on the RGB530 to 96 bits lets more data flow into the chip on every cycle. The extra bandwidth is needed to support triple 1024-word-by-8-bit palette RAMs and the triple 8-bit monotonic DACs that deliver the RGB signals. Like the 525, the 530 comes in a 208-lead PQFP package and supports 4-, 8-, 16-, and 24-bit pixel inputs, and 5/6/5 RGB and 8-bit grey scale outputs. Other features include a 16-entry attribute table and a display timing generator so users can perform color overlays or underlays. The large on-chip palette RAMs and attribute table allow programmers to perform pixel-by-pixel selection of the color palette, as well as double and quad-buffer and pixel format with up to an 8-bit overlay or underlay. This greatly reduces overheads in the multiple-window client-server graphics environment. Hardware support for both cross-hair and 64-by-64-pixel cursors is included on the RGB530.

At the high end, the RGB561 satisfies the most feature-rich graphics requirements for mid-range to high-end workstations. The chip includes the same triple 1024-by-8-bit palette RAMs as on the 530, but designers added one more bit to each DAC, providing triple 9-bit monotonic DACs. The wider DACs provide a better color continuum with up to 134 million colors. The memory interface bus was widened to 200 bits, more than doubling the video data that can be transferred each cycle. The port allows pixel interleaves and multiplexing ratios of 4:1, 5:1, or 8:1. The wide bus also pushes the circuit pin-count up—the RGB561 will come in a 304-lead quad-sided flat package.

The attribute table was upped to two sets of 256 entries, so programmers have plenty of memory for pixel-by-pixel selection of pixel format, color palette, color mode, and gamma correction for both primary and overlay data. To produce high-quality images, the 561 also packs independent gamma correction, which is used to improve the display linearity. Gamma coefficients would be loaded into the gamma palette's memory. Samples of the RGB525 and 530 are available now; the 561 will be available next month. In lots of 10,000, the 170-MHz version of the 530 and 561 sell for $71 and $103 each, respectively; the 250-MHz versions will cost $116 and $194 each, in 10,000-unit lots, and the RGB525 is $52 or $83 each, respectively, for the 170- and 250-MHz versions.

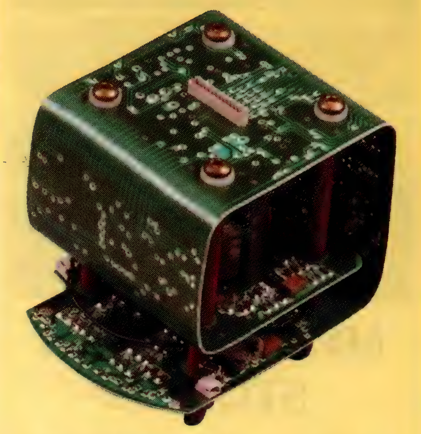
IBM Microelectronics, Route 100, P.O. Box 100, Somers, NY 10589; Mike West, (800) 426-0181.

CIRCLE 932

FAST PAGE-MODE DRAMS SUBSTITUTE FOR VRAMS

With a fast-page mode transfer time of 25 ns/byte, the 2-Mbit V53C8256—a 256-kword-by-8-bit dynamic RAM—delivers performance comparable to expensive video RAMs. Thus, the high-speed DRAMs provide a low-cost solution for high-performance VGA and other graphics subsystems. Just four of the 256k-by-8 DRAMS can replace either eight 256k-by-4 DRAMs or four 256k-by-8 VRAMs and reduce memory cost by 50% or more. The 53C8256 has a fast normal-access mode that allows standard random accesses to take place in just 45 ns (first access to any page). The DRAMs come in two refresh options and two power supply choices—the V53C8256H and N have an 8-ms refresh interval and operate from a 5-V supply, while the 8256HL and NL have a 64-ms interval and operate from a 3.3-V supply. The 5-V parts offer the 45-ns access time and 25-ns fast page mode; the 3.3-V parts have a 60-ns/45-ns access/fast-page transfer speeds. The 5-V versions draw 160 mA when active and as little as 1 mA on standby (H suffix); the HL low-power version reduces the 5-V standby drain to just 0.15 mA. The 3.3-V versions draw half or less than the current levels of the 5-V parts. Prices for the V53C8256 start at $8 each in volume for the 5-V H- or 3-V N-suffix versions (24-pin DIP or 24- or 26-lead 300-mil SOJ packages). Both are available from stock. The HL or NL versions can be special ordered.

Mosel-Vitelic, 3510 N. First St., San Jose, CA 95134-1501; (408) 433-6025. **CIRCLE 933**



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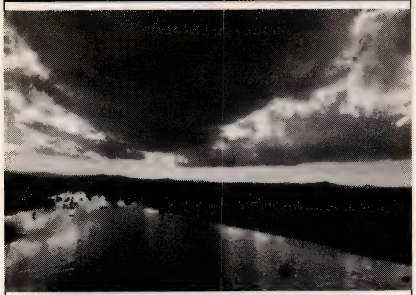

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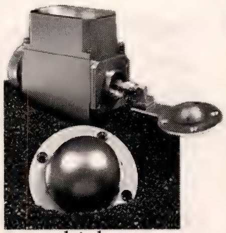

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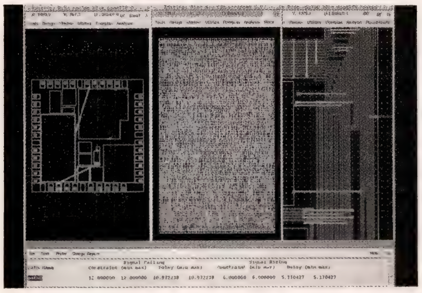
VHDL SIMULATOR RUNS FASTER AT ALL LEVELS

The latest version of the Synopsys VHDL System Simulator (VSS) speeds simulation at all levels, including behavior, register-transfer level, and gates. Version 3.1 of VSS combines multiple simulation technologies, support from ASIC vendors for VHDL sign-off, and a smooth migration path from Verilog to VHDL. Compiled, interpreted, and optimized gate-level simulation technologies are combined in the new software to provide up to 10 times the simulation speed of the company's Version 3.0 VSS. Version 3.0 provided interpreted simulation focused on debugging. Also, VSS is the first VHDL simulator to be given golden or sign-off capability with an ASIC vendor. NEC Electronics announced that they are working with Synopsys to develop VSS for ASIC sign-off. To achieve sign-off capability, a simulator must have submicron-accurate timing, glitch handling, and post-layout back-annotation. VSS Version 3.1 will ship by the end of the year. It runs on Unix workstations, and costs $24,000. LM

Synopsys Inc., 700 E. Middlefield Rd., Mountain View, CA 94043-4033; (415) 962-5000. **CIRCLE 934**

TURBO OPTION BEEFS UP VERILOG-XL SIMULATOR



Cadence now offers a choice of two Verilog products to provide designers flexibility when configuring their top-down environments. A new Turbo version of the Verilog-XL digital-logic simulator gives users more speed than the current version 1.7 Verilog, along with improved efficiency and ease-of-use. Verilog-XL Turbo is a high-end package that's actually a superset of the existing Verilog-XL product. On the average, it can simulate at the behavioral level seven times faster than the current product, yet is completely compatible with it. The Verilog-XL Turbo environment includes a language-sensitive editor for correct-by-construction code entry, a language analyzer/parser for syntax checking, color-coded syntax readability, and the ability to annotate error messages directly to source code. In addition, Turbo's debug environment has improved graphical features such as a signal-flow browser and a powerful new standalone waveform tool. Finally, Turbo delivers better memory utilization, allowing designers to run larger designs in less space. In fact, the enhancement reduces the amount of memory used by up to three times. Pricing for the Verilog-XL Turbo and existing version 1.7 simulators start at $32,000 and $20,000, respectively. Both products are shipping now. The simulators run on Unix-based workstations. LM

Cadence Design Systems Inc., 555 River Oaks Pkwy., San Jose, CA 95134; (408) 943-1234. **CIRCLE 935**

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Import Export Kernel is a software tool that provides a reverse-engineering path for designers who need to use existing pc-board design data in the Mentor Graphics environment. The system will convert pc-board artwork in Gerber or IPC-D-350 formats, pc-board data in EDIF files, or pc-board designs from eight major CAD tools into software that can be used with Mentor Graphics tools. In addition, Import Export Kernel improves board manufacturability with test-point generation, design-rule checks, and interactive visual artwork verification. The system runs on Unix workstations under a Motif-based interface. Call the company for pricing and additional information. LM

Intercept Technology Inc., 1819 Peachtree Rd. NE, Suite 611, Atlanta, GA 30309-1859; (404) 352-3744. **CIRCLE 936**

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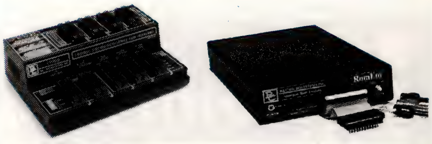

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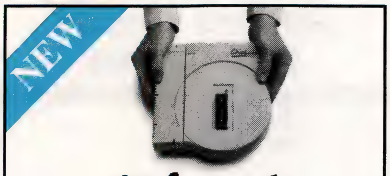

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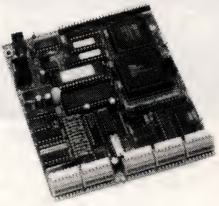

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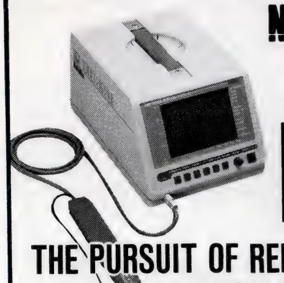

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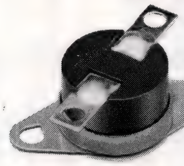

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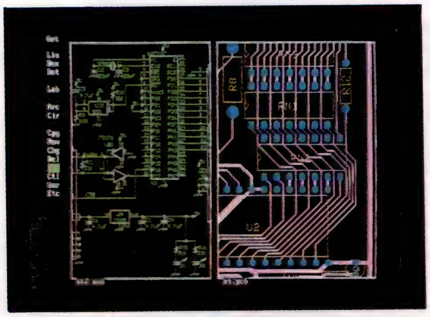

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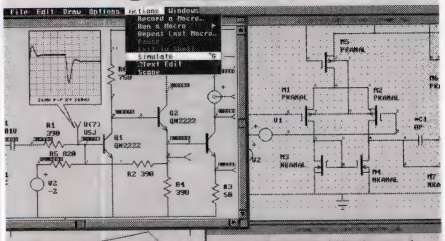

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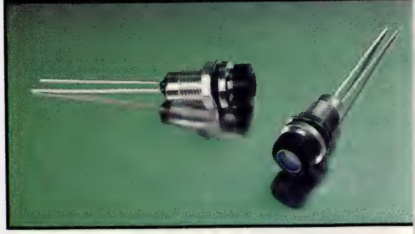

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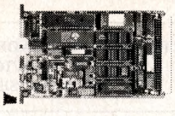

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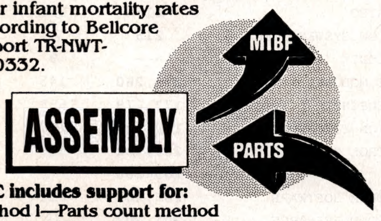

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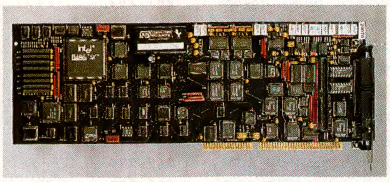

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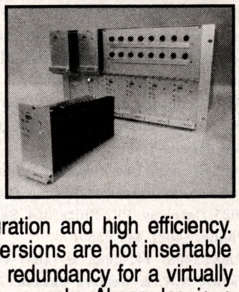

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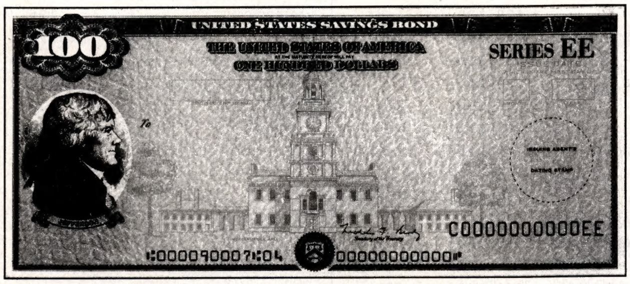

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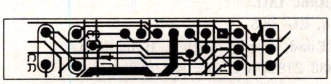

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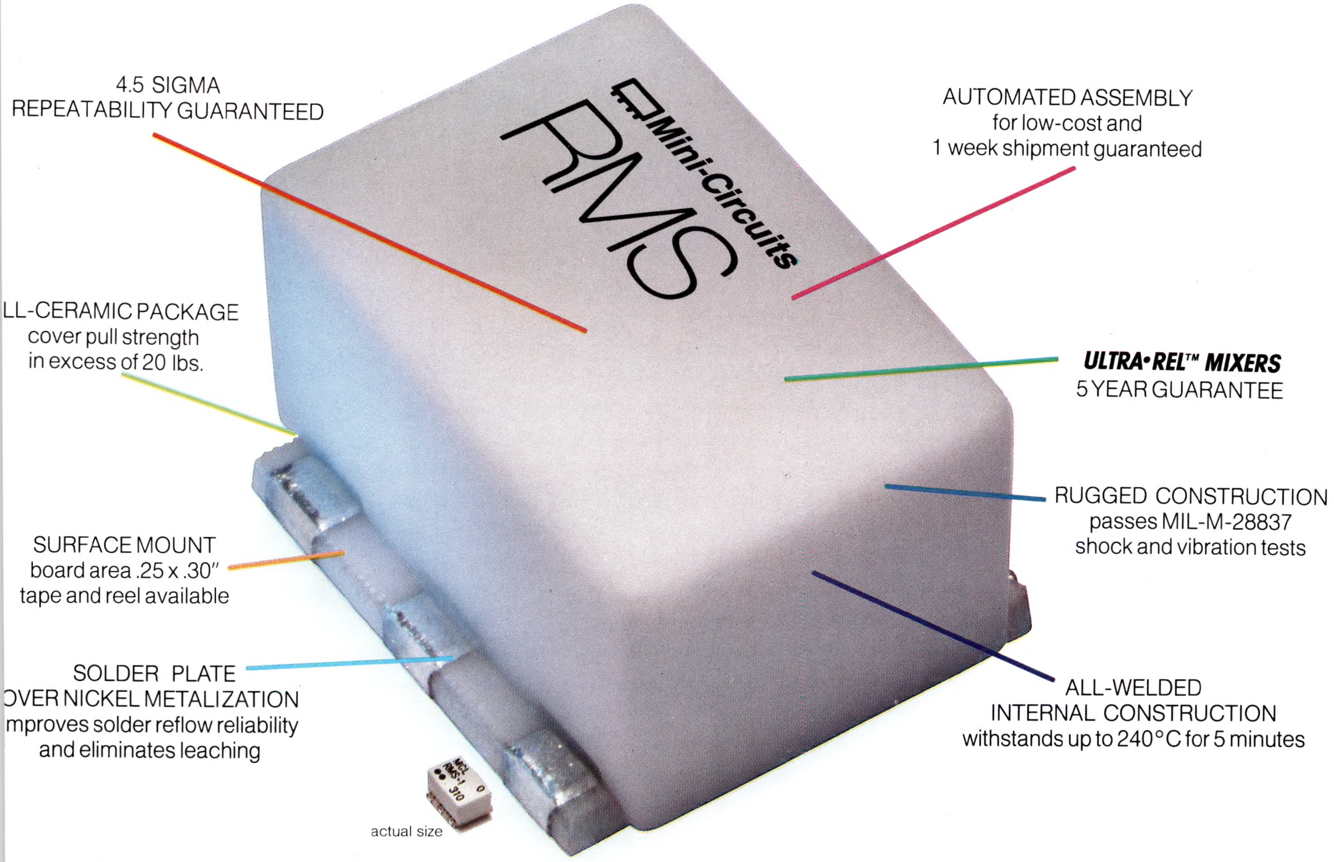

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